

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,J45

DVT 8/6/2013

Page

(.cma)

Contents

Sync

Date

1

Table of Contents

MASTER

10/25/2012

2

BOM Configuration

J15_MLB

10/31/2012

3

BOM Configuration

J15_MLB

10/31/2012

4

PD Parts

J15_MLB

12/18/2012

5

CPU DMI/PEG/FDI/RSVD

J15_REFERENCE

12/18/2012

6

CPU Clock/Misc/JTAG/CFG

J15_REFERENCE

12/18/2012

7

CPU DDR3 Interfaces

J15_REFERENCE

12/18/2012

8

CPU Power

J15_REFERENCE

12/18/2012

9

CPU Ground

J15_REFERENCE

12/18/2012

10

CPU Decoupling

J15_REFERENCE

12/18/2012

11

PCH RTC/HDA/JTAG/SATA/CLK

J15_REFERENCE

12/18/2012

12

PCH DMI/FDI/PM/GFX/PCI

J15_REFERENCE

12/18/2012

13

PCH PCI-E/USB

J15_REFERENCE

12/18/2012

14

PCH GPIO/MISC/NCTF

J15_REFERENCE

12/18/2012

15

PCH Power

J15_REFERENCE

12/18/2012

16

PCH Grounds

J15_REFERENCE

12/18/2012

17

PCH DECOUPLING

J15_REFERENCE

12/18/2012

18

CPU & PCH XDP

J15_MLB

12/18/2012

19

Chipset Support

J15_REFERENCE

01/14/2013

20

Project Chipset Support

J15_REFERENCE

12/18/2012

21

CPU Memory S3 Support

J15_REFERENCE

10/31/2012

22

DDR3 VREF MARGINING

J15_MLB

10/31/2012

23

DDR3 SDRAM Bank A (1 OF 2)

J15_MLB

10/31/2012

24

DDR3 SDRAM Bank A (2 OF 2)

J15_MLB

10/31/2012

25

DDR3 SDRAM Bank B (1 OF 2)

J15_MLB

10/31/2012

26

DDR3 SDRAM Bank B (2 OF 2)

J15_MLB

10/31/2012

27

DDR3 Termination

J15_MLB

01/14/2013

28

Thunderbolt Host (1 of 2)

T29_RR

01/14/2013

29

Thunderbolt Host (2 of 2)

T29_RR

01/14/2013

30

Thunderbolt Mobile Support

T29_RR

12/18/2012

31

Thunderbolt Connector A

J15_REFERENCE

12/18/2012

32

Thunderbolt Connector B

J15_REFERENCE

11/16/2012

33

DDC Crossbar

J15_REFERENCE

10/31/2012

34

X29C CONNECTOR

J15_MLB

06/08/2013

35

SSD Connector

CLEAN_MLB_KEPLER

06/13/2013

36

Camera 1 of 2

CLEAN_MLB_KEPLER

06/13/2013

37

Camera 2 of 2

CLEAN_MLB_KEPLER

10/31/2012

38

USB 3.0 CONNECTORS

J15_MLB

03/15/2013

39

KEYBOARD/TRACKPAD (1 OF 2)

CHANG_J45

03/15/2013

40

KEYBOARD/TRACKPAD (2 OF 2)

CHANG_J45

03/15/2013

41

SMC

CHANG_J45

Page

(.cma)

Contents

Sync

Date

42

SMC Shared Support

CHANG_J45

03/15/2013

43

SMC Project Support

CHANG_J45

11/26/2012

44

SMBus Connections

CHANG_J45

12/21/2012

45

High Side Voltage and Current Sensing

CHANG_J45

03/15/2013

46

Load Side Voltage and Current Sensing

CHANG_J45

12/21/2012

47

Debug Sensors

CHANG_J45

11/26/2012

48

Thermal Sensors

CHANG_J45

10/31/2012

49

Fan Connectors

J15_MLB

10/31/2012

50

SPI ROM / LPC+SPI Conn.

J15_MLB

07/30/2013

51

AUDIO:CODEC, ANALOG

JOB_J45

07/30/2013

52

AUDIO:CODEC, DIGITAL

JOB_J45

07/30/2013

53

AUDIO: SPEAKER AMP

JOB_J45

07/30/2013

54

AUDIO: JACK

JOB_J45

07/30/2013

55

AUDIO: JACK TRANSLATORS

JOB_J45

10/31/2012

56

DC-In & Battery Connectors

J15_MLB

10/31/2012

57

PBus Supply & Battery Charger

J15_MLB

10/31/2012

58

CPU VR12.5 VCC Regulator IC

J15_MLB

10/31/2012

59

CPU VR12.5 VCC Power Stage

J15_MLB

10/31/2012

60

1.35V DDR3L SUPPLY

J15_MLB

10/31/2012

61

5V / 3.3V Power Supply

J15_MLB

10/31/2012

62

1V05V POWER SUPPLY

J15_MLB

06/13/2013

63

LCD/KBD Backlight Driver

CLEAN_MLB_KEPLER

10/31/2012

64

Misc Power Supplies

J15_MLB

10/31/2012

65

Power FETs

J15_MLB

03/15/2013

66

Power Control 1/ENABLE

CHANG_J45

10/31/2012

67

eDP Display Connector

J15_MLB

10/31/2012

68

RIO Connectors

J15_MLB

10/31/2012

69

Power Aliases

J15_MLB

10/31/2012

70

Signal Aliases

J15_MLB

10/31/2012

71

Functional Test Points

J15_MLB

10/31/2012

72

NC & No Test

J15_MLB

12/10/2012

73

PCB Rule Definitions

SIDLE_J45

12/10/2012

74

CPU Constraints

SIDLE_J45

12/10/2012

75

PCH Constraints 1

SIDLE_J45

12/10/2012

76

PCH Constraints 2

SIDLE_J45

12/10/2012

77

Memory Constraints

SIDLE_J45

12/10/2012

78

Thunderbolt Constraints

SIDLE_J45

12/10/2012

79

Camera Constraints

SIDLE_J45

12/10/2012

80

SMC Constraints

SIDLE_J45

12/10/2012

81

Project Specific Constraints

SIDLE_J45

REV

ECN

DESCRIPTION OF REVISION

CK APPD

DATE

<REV>

<ECN>

<ECO_DESCRIPTION>

<ECODATE>

8

7

6

5

4

3

2

1

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0456	1	SCHEM,MLB,J45	SCH	CRITICAL	
820-3662	1	PCB,MLB,J45	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=ABBREV

LAST_MODIFIED=Thu Aug 6 17:09:28 2013

DRAWING TITLE

<PART_DESCRIPTION>

Apple Inc.

Apple

DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

BRANCH

<BRANCH>

PAGE

1 OF 118

SHEET

1 OF 81

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

8

7

6

5

4

3

2

1

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB,J45	J45_COMMON
985-0045	DEV BOM,MLB,J45	J45_DEVEL:ENG
639-4822	PCBA,MLB,BETTER,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE,COMMON,J45_COMMON1,J45_COMMON2,J45_PROGPARTS
J45_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUEG:X16,S2_PWR:S0
J45_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45_PVB	BKLT:PROD,SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT,TBTROM_PROG:DVT,TBTROM:PROG,TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE,XDP_DEBUG,SOPGOOD_ISL,DDRREF_DAC,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW, SR187, FRQ, C0, 2.0, 47W, 4+3E, 6M, BGA	U0500	CRITICAL	CPU_CRW: BETTER
337S4600	1	CRW, SR188, FRQ, C0, 2.3, 47W, 4+3E, 6M, BGA	U0500	CRITICAL	CPU_CRW: BEST
337S4624	1	CRW, SR189, FRQ, C0, 2.6, 47W, 4+3E, 6M, BGA	U0500	CRITICAL	CPU_CRW: CTO
337S4542	1	IC, QCRW, LST-M, KM87, C2, SR199, FPG, FCNGA	U1100	CRITICAL	
338S1247	1	IC, TWT, FR-4C, A0, FRQ, C10, SR13C, FCNGA288	U2800	CRITICAL	
338S1186	1	IC, BCM15700A2, S2, PCIE CNRA, 8XS, 208PFCBGA	U3900	CRITICAL	
333S0700	1	IC, SDRAM, 4GBIT, DDR3L-1600, GEMMA, 96B FBGA	U4000	CRITICAL	
333S0667	16	IC, SDRAM, 4GBIT, DDR3L-1600, HUNGA, 78P FBGA		CRITICAL	HYNIX_1600_S
333S0624	16	IC, SDRAM, DDR3-1600, 512MX8, 78PFBGA, C-DIE, SAMSUNG		CRITICAL	SAMSUNG_1600_S
333S0703	16	IC, SDRAM, 4GBIT, DDR3L-1600, F, DIE, RS, 78P		CRITICAL	ELPIDA_1600_S
333S0660	16	IC, SDRAM, 4GBIT, DDR3L-1600, V80A, 78P, FBGA		CRITICAL	MICRON_1600_S
333S0667	32	IC, SDRAM, 4GBIT, DDR3L-1600, HUNGA, 78P FBGA		CRITICAL	HYNIX_1600
333S0624	32	IC, SDRAM, DDR3-1600, 512MX8, 78PFBGA, C-DIE, SAMSUNG		CRITICAL	SAMSUNG_1600
333S0703	32	IC, SDRAM, 4GBIT, DDR3L-1600, F, DIE, RS, 78P		CRITICAL	ELPIDA_1600
333S0660	32	IC, SDRAM, 4GBIT, DDR3L-1600, V80A, 78P, FBGA		CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L
RAM:MICRON_1600	MICRON_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=J15 MLB		SYNC DATE=10/25/2012	
PAGE TITLE			
BOM Configuration			
 Apple Inc.		DRAWING NUMBER	
		<SCH_NUM>	
		SIZE	
		D	
		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		<BRANCH>	
		PAGE	
		2 OF 118	
		SHEET	
		2 OF 81	

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Spacm Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Spacm
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cytotec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to Om Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cytotec alt to PPT
376S1032	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NDP alt to Diodes
376S1089	376S1128		ALL	NDP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elpida F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba (U2036, U7001)

Programmables - All builds

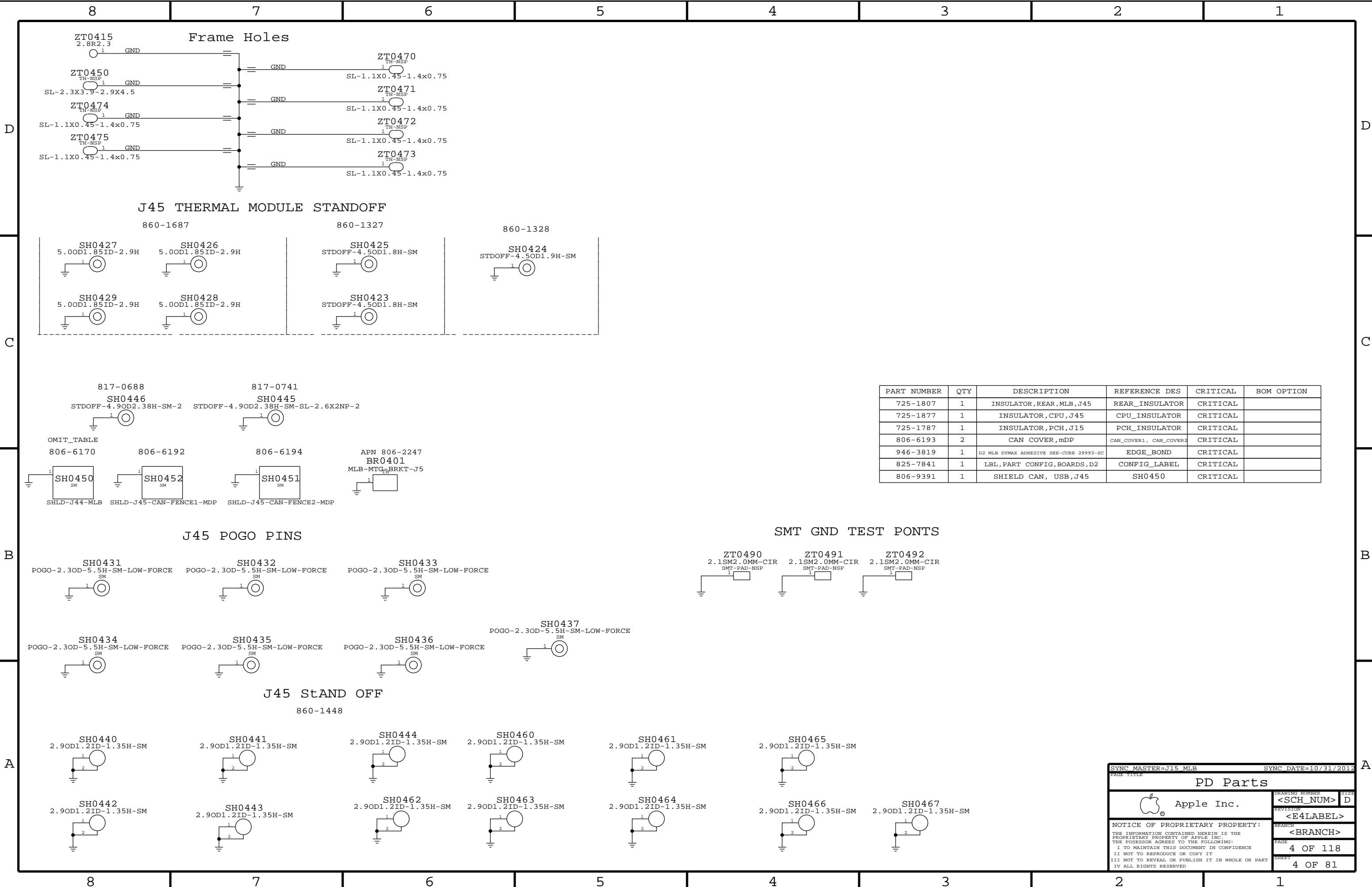
335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S3919	1	IC,EPROM,Falcon RIDGE(V13.9)J44/45	U2890	CRITICAL	TBTROM:PROG
337S4587	1	IC,TP PSOC, QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK
341S3856	1	IC,TRKPD/KYBD,PSOC(V225)	U4801	CRITICAL	TPAD_PSOC:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL_FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC,SMC-B1,EXT,V2.12A54,EVT,J45	U5000	CRITICAL	SMC_PROG:EVT
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC,SPI SRL 50MHZ FLASH,64MBIT,SOIC8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC,EFI ROM(VXXXX)PROTO 0,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC,EFI ROM(V0035)PRE-PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PRE-PROTO1
341S3793	1	IC,EFI ROM(V0041)PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC,EFI ROM(V00xx)PROTO 2,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC,EFI ROM(V0100)PROTO3-J45 &EVT-J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC,EFI ROM(Vxxxx)DVT-J45	U6100	CRITICAL	BOOTROM_PROG:DVT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR, REAR, MLB, J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR, CPU, J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR, PCH, J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER, mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL, PART CONFIG, BOARDS, D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB, J45	SH0450	CRITICAL	

SYNC MASTER=J15 MLB

SYNC DATE=10/31/2012

PD Parts

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

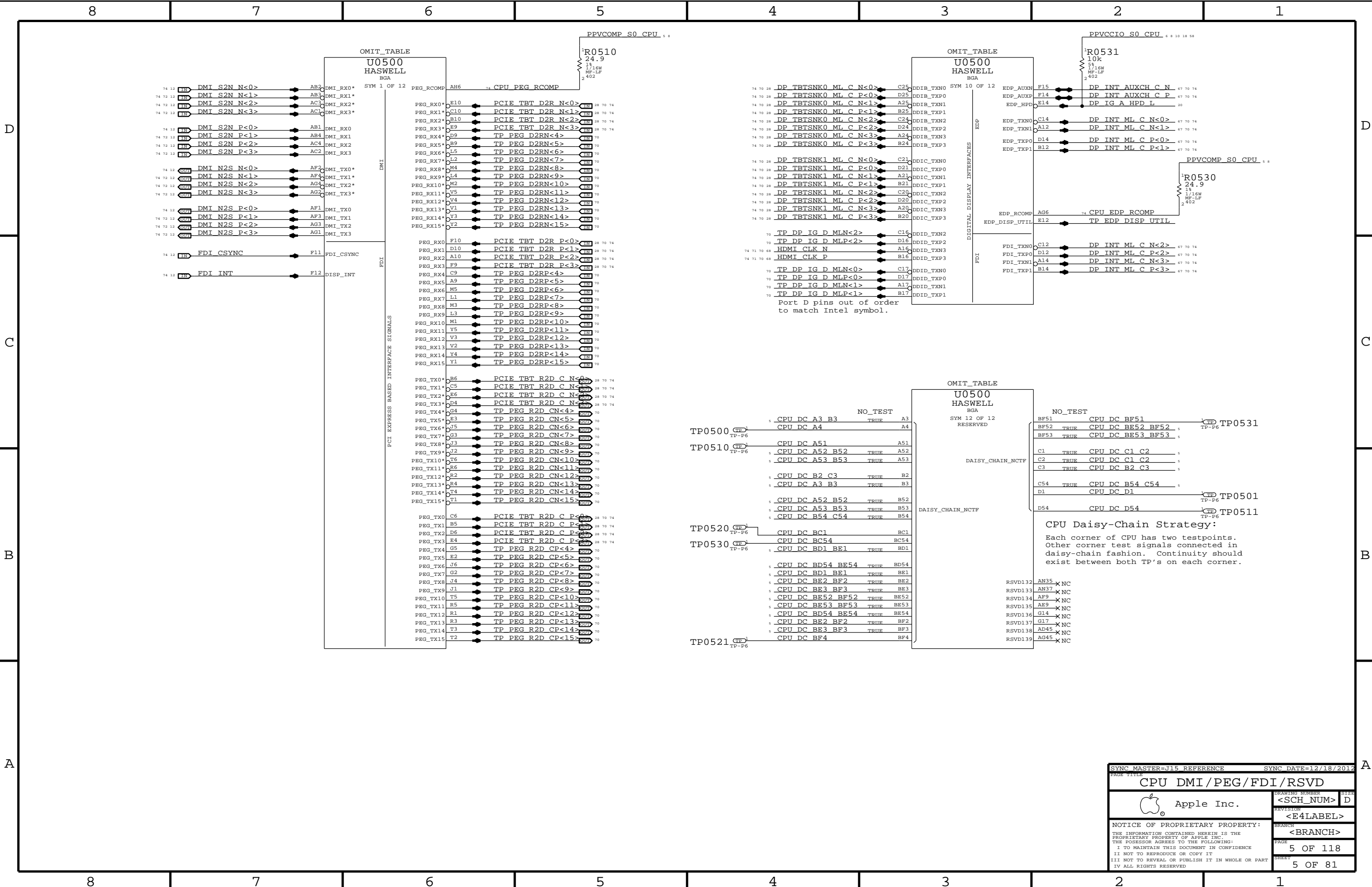
DRAWING NUMBER
<SCH_NUM> D

REVISION
<E4LABEL>

BRANCH
<BRANCH>

PAGE
4 OF 118

SHEET
4 OF 81



Port D pins out of order to match Intel symbol.

CPU Daisy-Chain Strategy:
Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

D

C

B

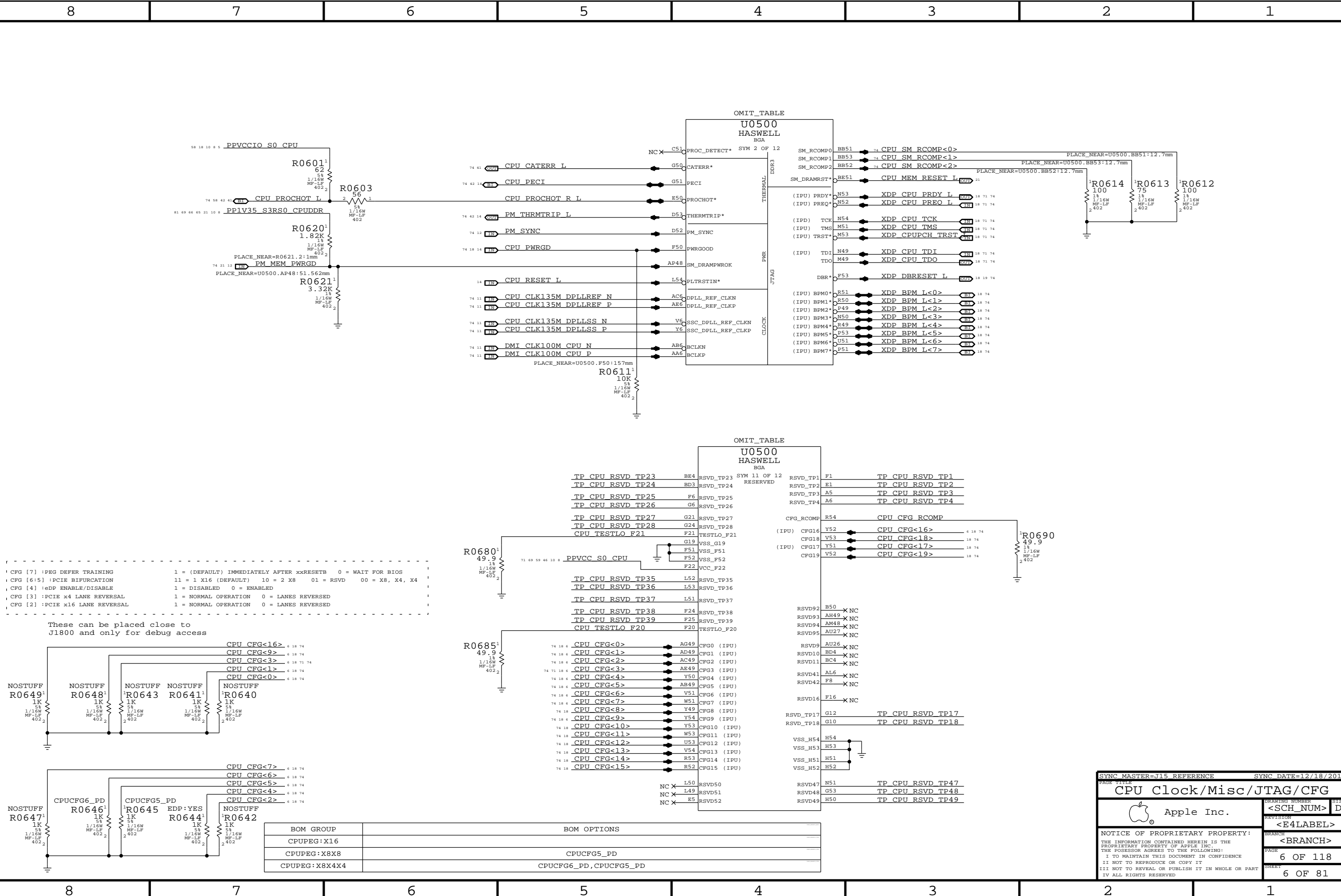
A

D

C

B

A



SYNC MASTER=J15 REFERENCE

SYNC DATE=12/18/2012

CPU Clock/Misc/JTAG/CFG

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED

DRAWING NUMBER

REVISION

BRANCH

PAGE

SHEET

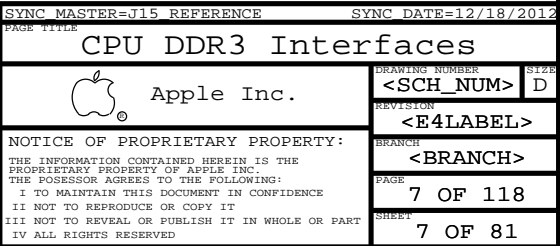
<SCH_NUM>

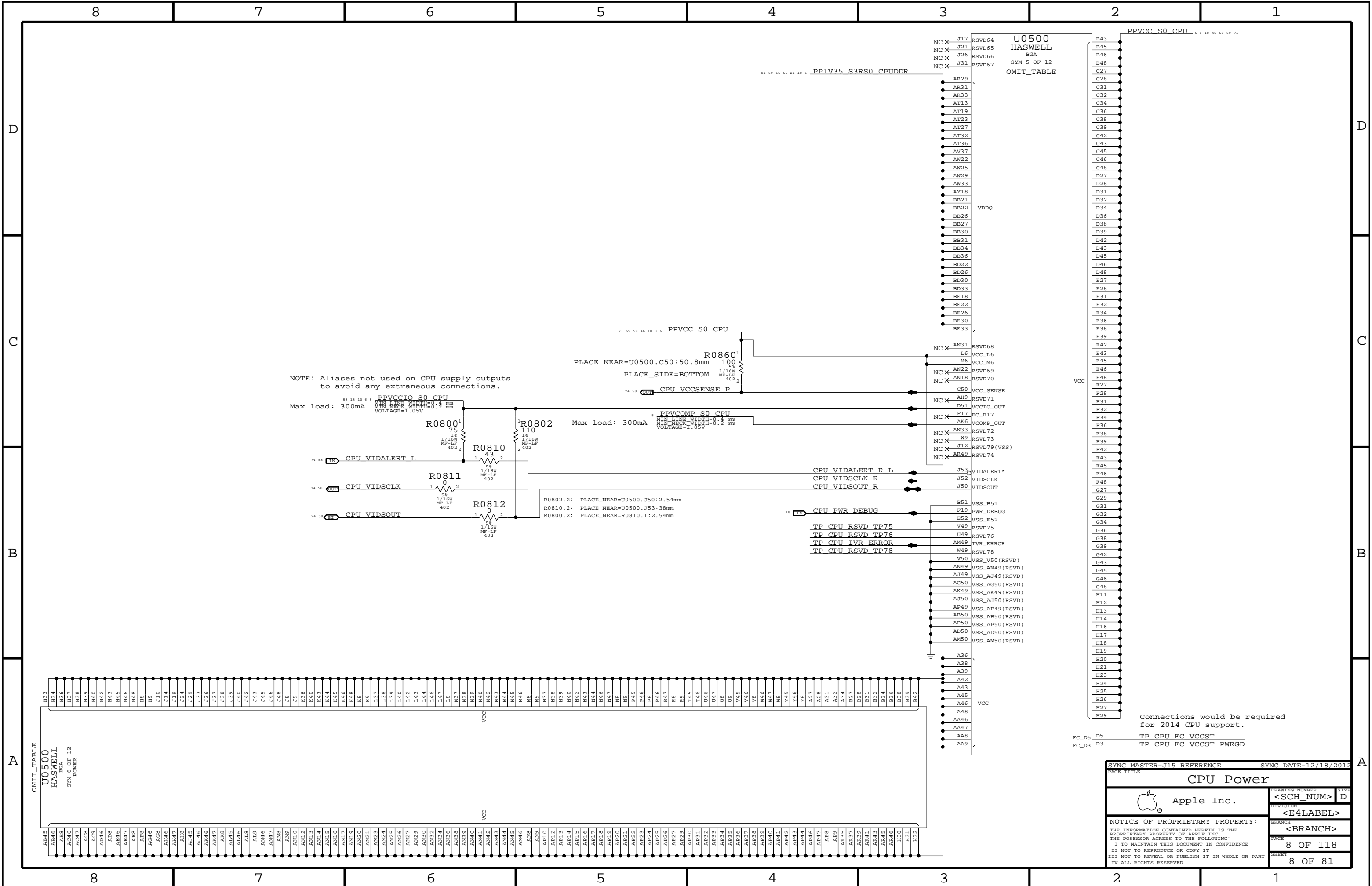
<E4LABEL>

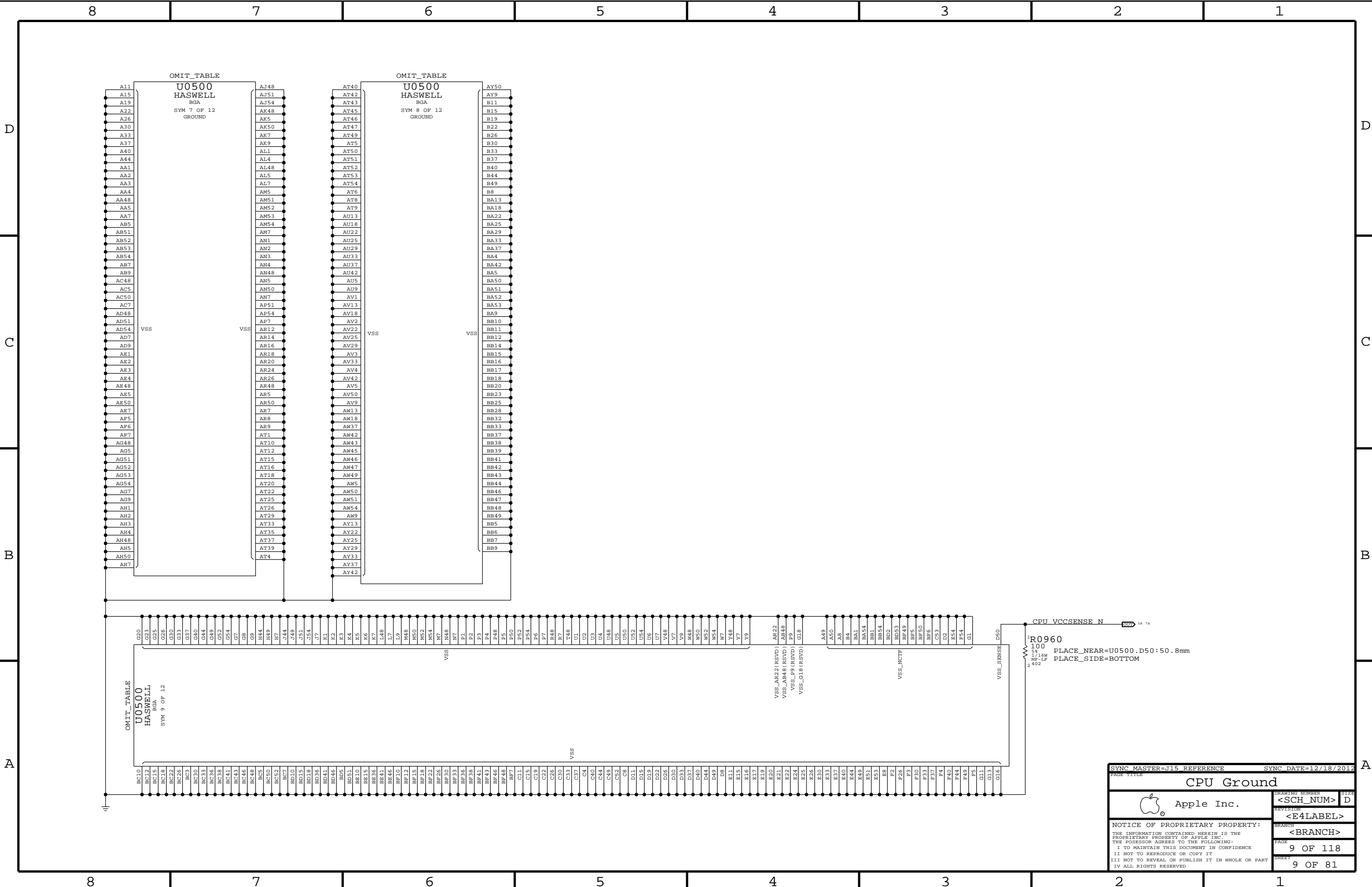
<BRANCH>

6 OF 118

6 OF 81





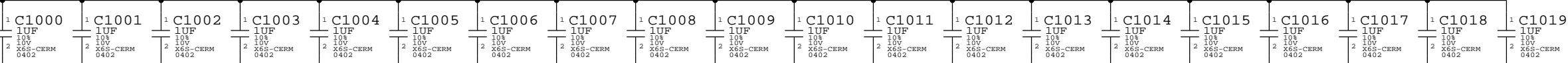


CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

PLACEMENT_NOTE (C1000-C1019):

Place on bottom side of U0500

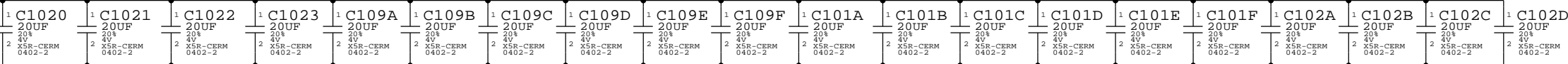


NO STUFF

PLACEMENT_NOTE (C1020-C1023):

CAPS for Acoustic control (C109A-C102D)

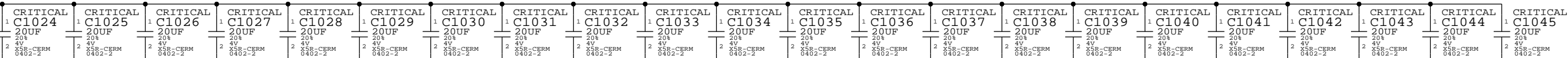
Place near U0500 on bottom side



NO STUFF

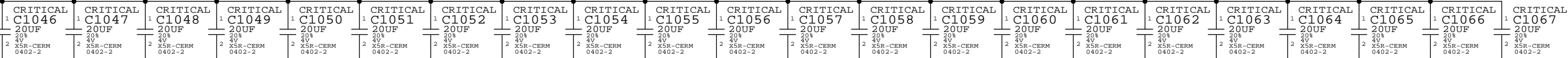
PLACEMENT_NOTE (C1024-C1045):

Place near inductors on bottom side.



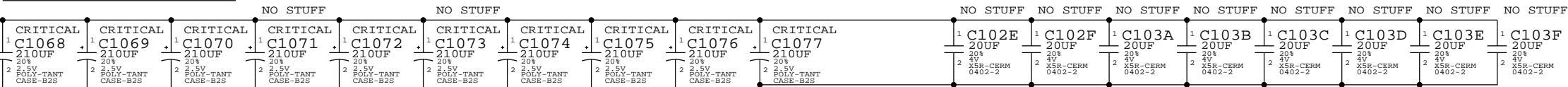
PLACEMENT_NOTE (C1046-C1067):

Place near inductors on bottom side.



PLACEMENT_NOTE (C1068-C1076):

CAPS for Acoustic control (C102E-C103F)

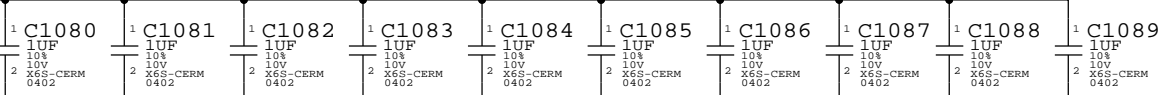


CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

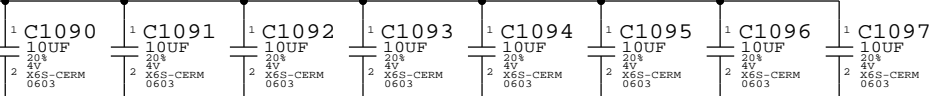
PLACEMENT_NOTE (C1080-C1089):

Place on bottom side of U0800

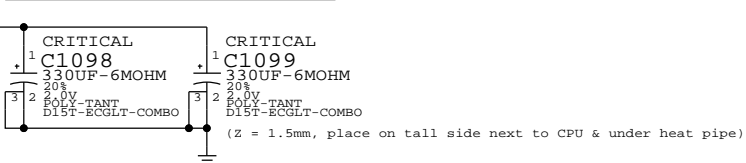


PLACEMENT_NOTE (C1090-C1097):

Place near U0500 on bottom side

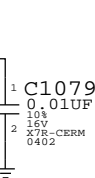


PLACEMENT_NOTE (C1098-C1099):




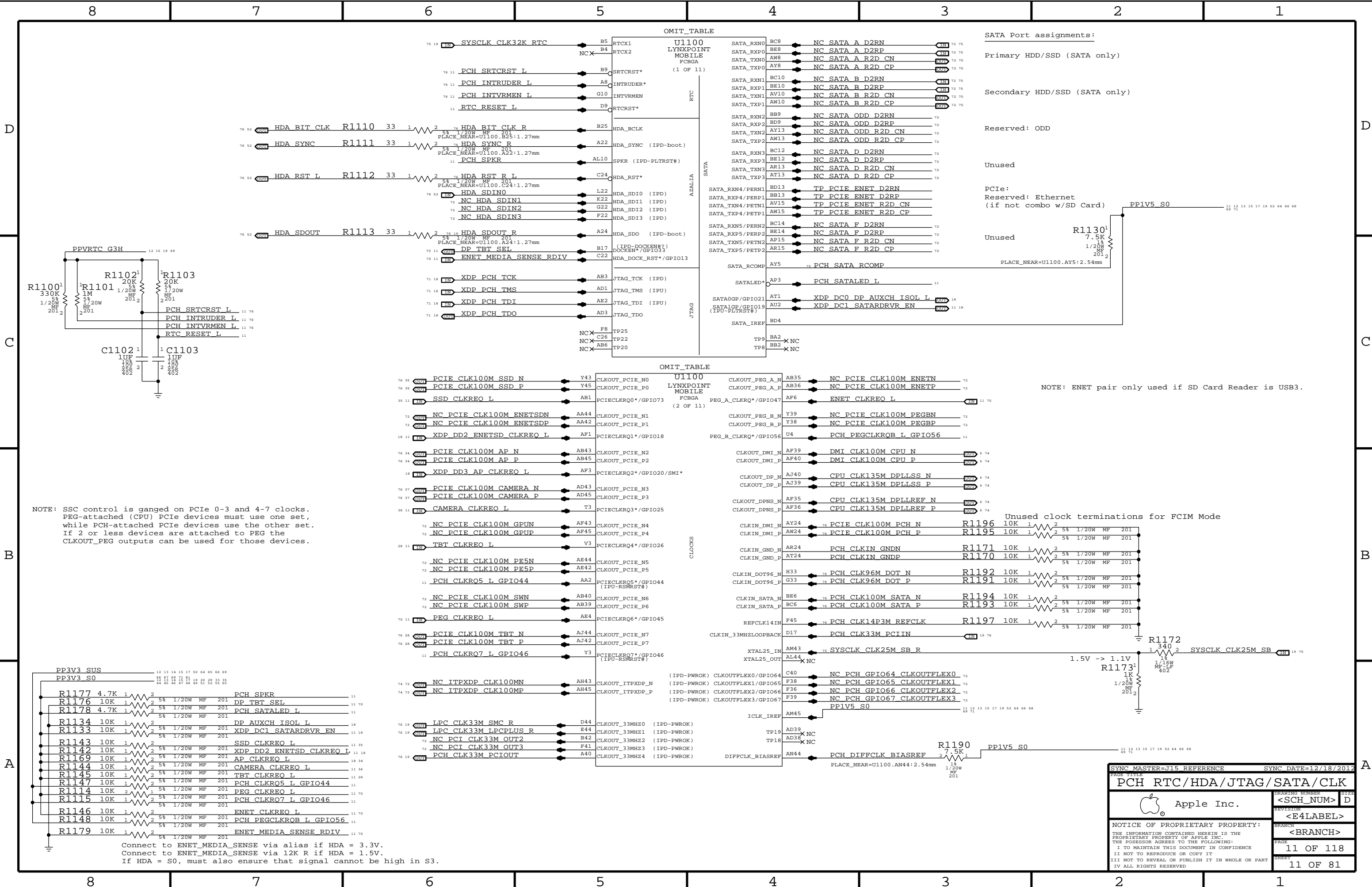
CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)



NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
CPU Decoupling			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	10 OF 118
		SHEET	10 OF 81



NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks. PEG-attached (CPU) PCIe devices must use one set, while PCH-attached PCIe devices use the other set. If 2 or less devices are attached to PEG the CLKOUT_PEG outputs can be used for those devices.

NOTE: ENET pair only used if SD Card Reader is USB3.

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC MASTER=J15 REFERENCE

SYNC DATE=12/18/2012

PCH RTC/HDA/JTAG/SATA/CLK

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

BRANCH

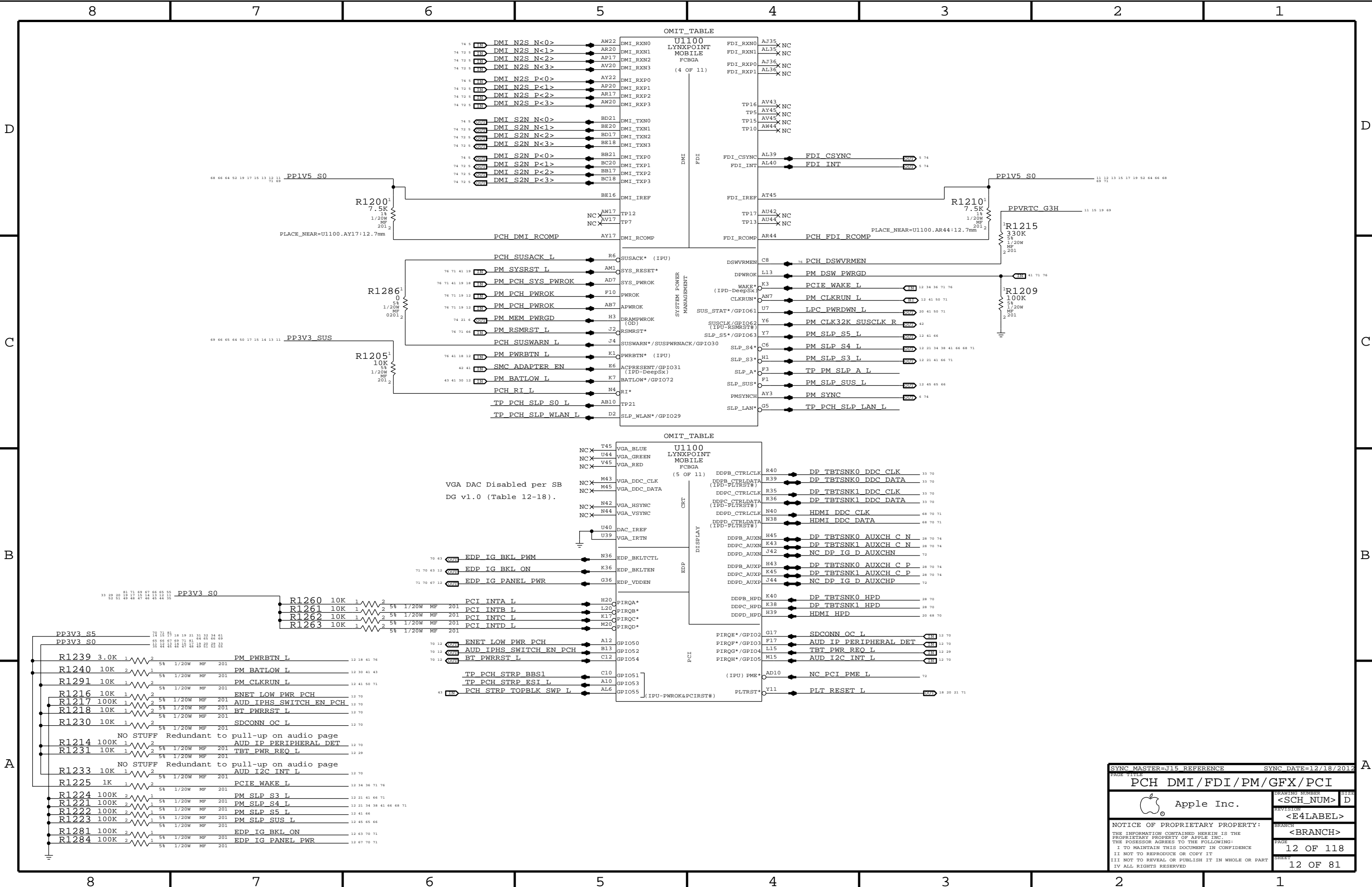
<BRANCH>

PAGE

11 OF 118

SHEET

11 OF 81




SYNC MASTER=J15 REFERENCE

SYNC DATE=12/18/2012

PAGE TITLE

PCH DMI / FDI / PM / GFX / PCI

 Apple Inc.

DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

BRANCH

<BRANCH>

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

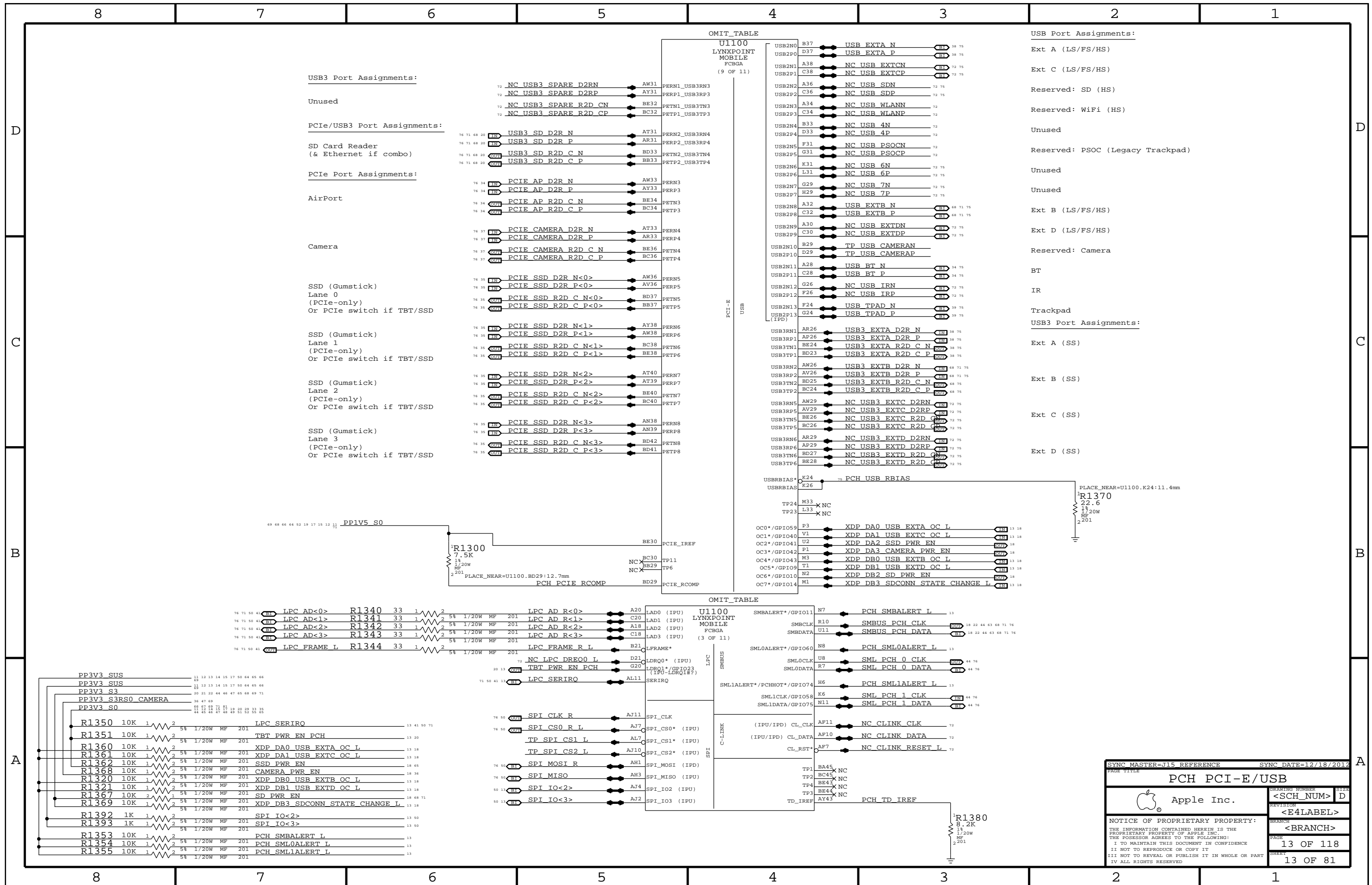
IV ALL RIGHTS RESERVED

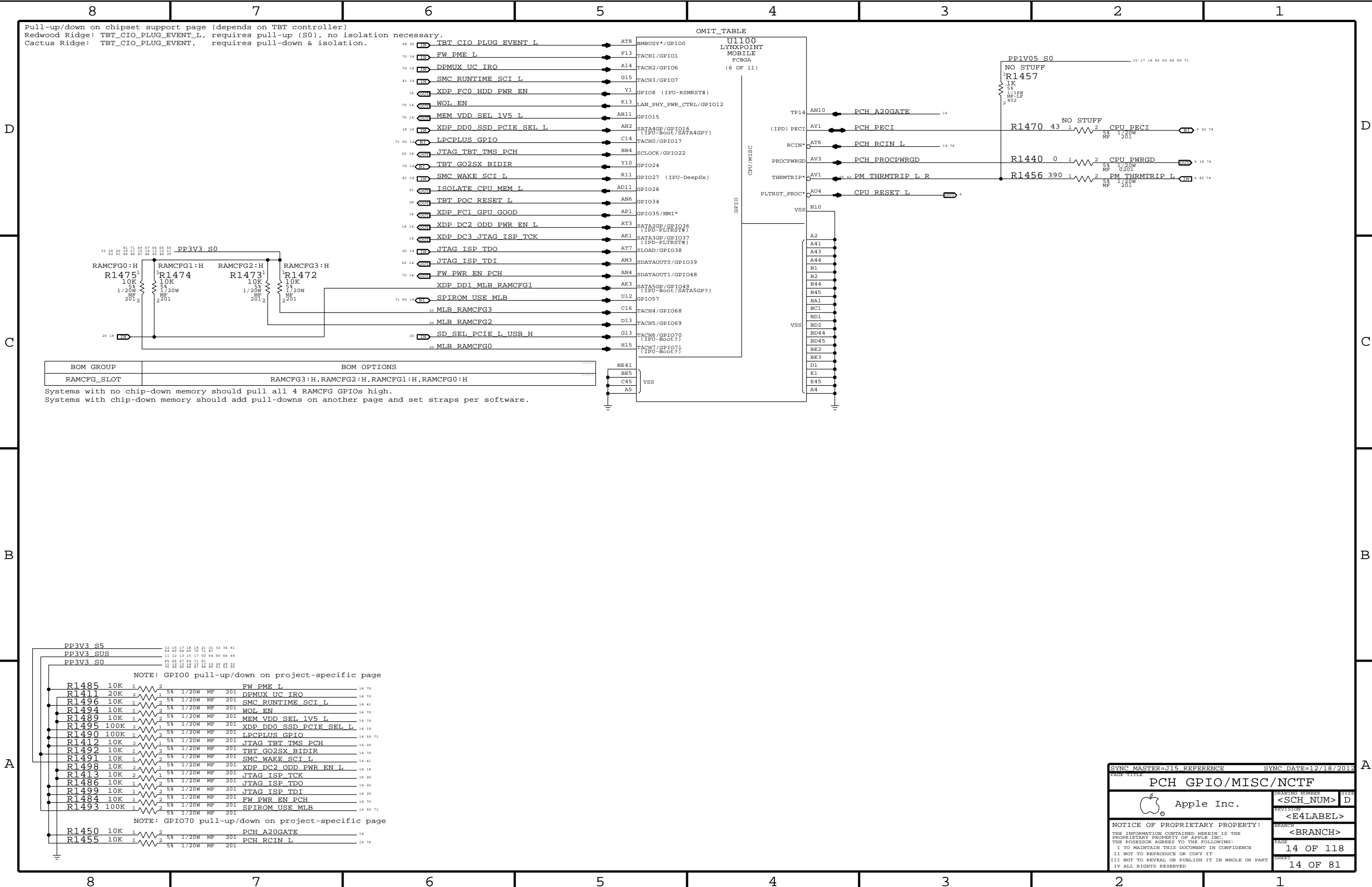
PAGE

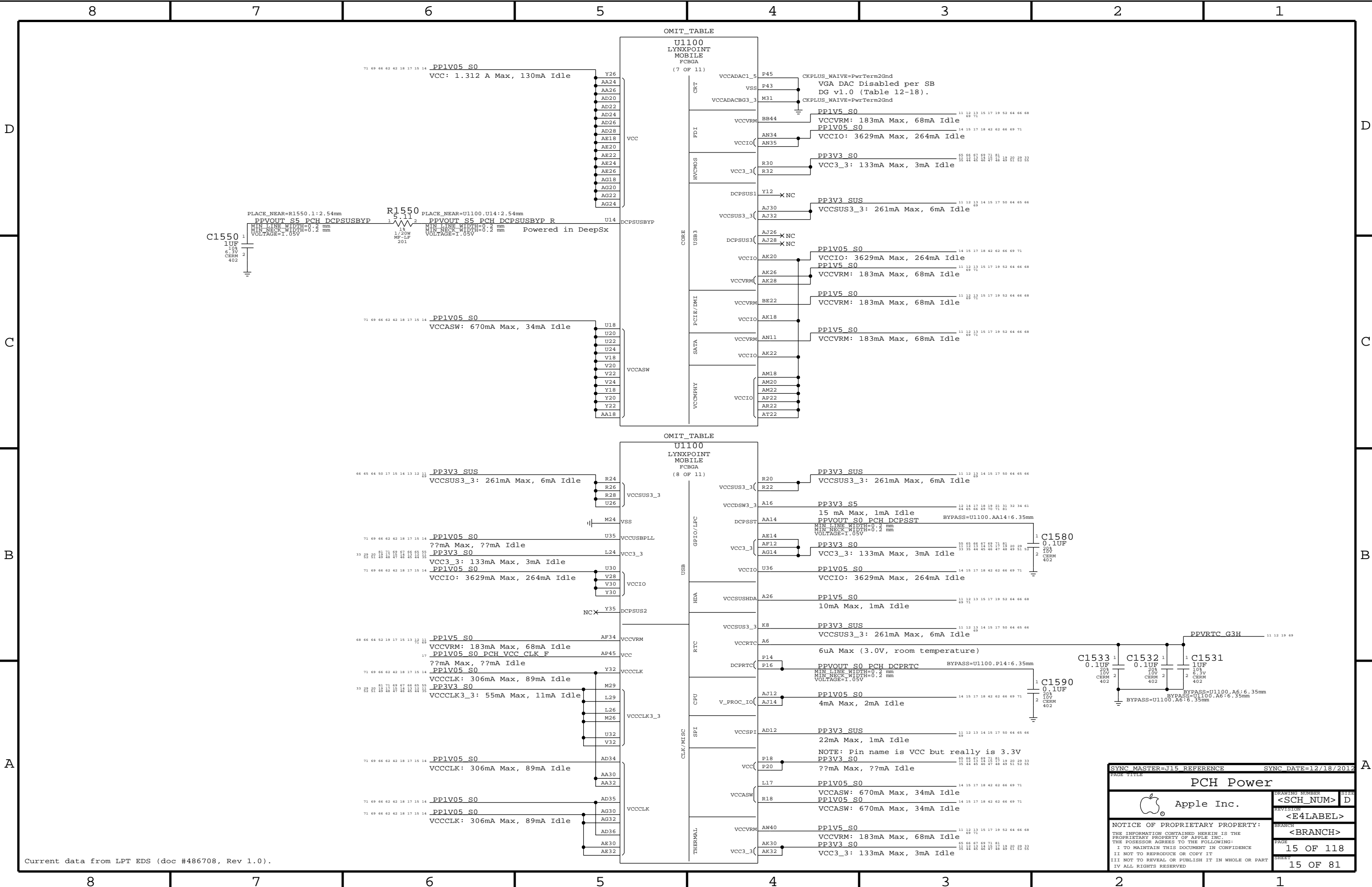
12 OF 118

SHEET


12 OF 81

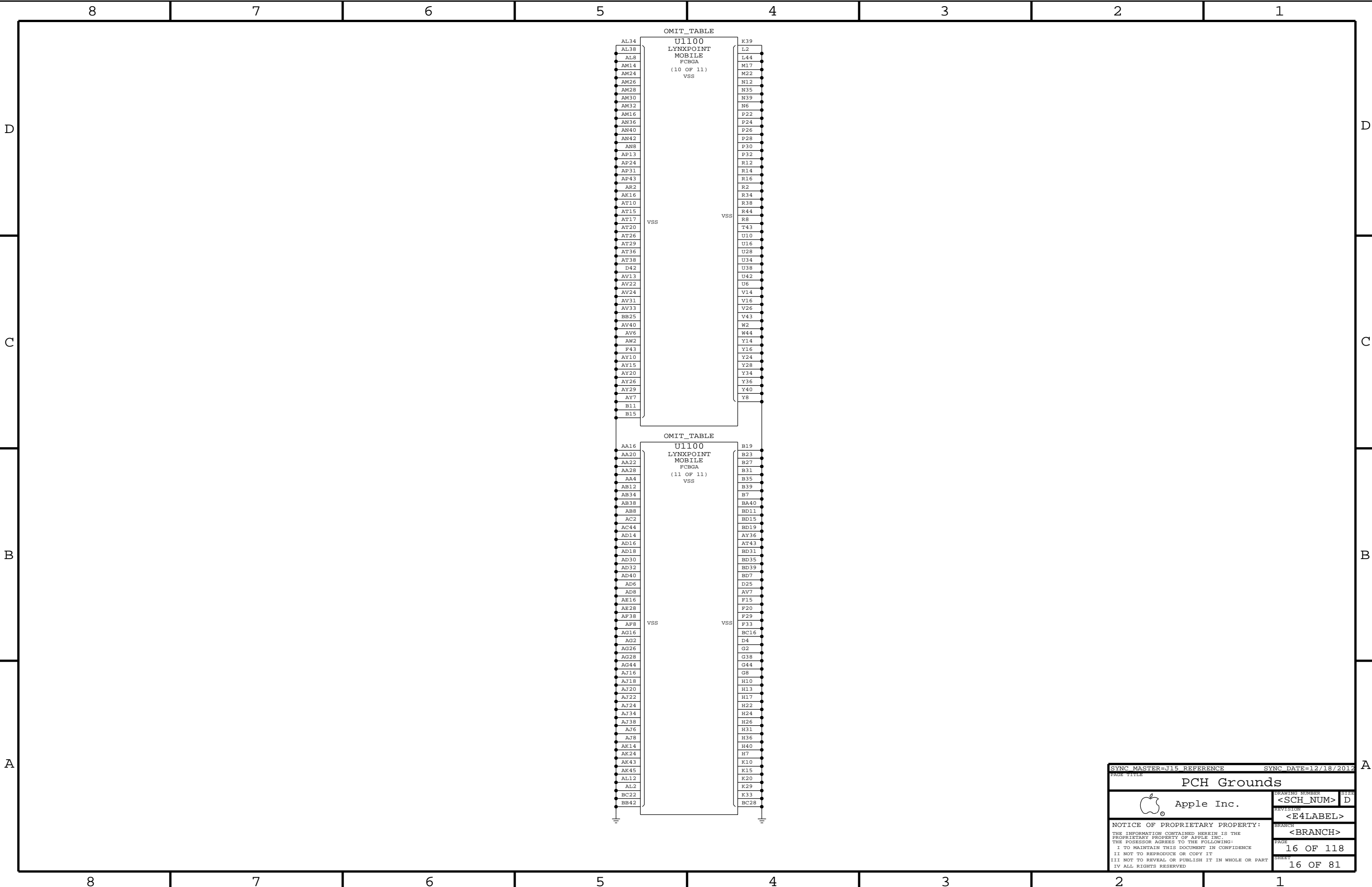






Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
PCH Power			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		<BRANCH>	
		PAGE	15 OF 118
		SHEET	15 OF 81



OMIT_TABLE

U1100
LYNXPPOINT
MOBILE
FCBGA
(10 OF 11)
VSS

AL34
AL38
AL8
AM14
AM24
AM26
AM28
AM30
AM32
AM16
AN36
AN40
AN42
AN8
AP13
AP24
AP31
AP43
AR2
AK16
AT10
AT15
AT17
AT20
AT26
AT29
AT36
AT38
D42
AV13
AV22
AV24
AV31
AV33
BB25
AV40
AV6
AW2
F43
AY10
AY15
AY20
AY26
AY29
AY7
B11
B15

VSS

VSS

K39
L2
L44
M17
M22
N12
N35
N39
N6
P22
P24
P26
P28
P30
P32
R12
R14
R16
R2
R34
R38
R44
R8
T43
U10
U16
U28
U34
U38
U42
U6
V14
V16
V26
V43
W2
W44
Y14
Y16
Y24
Y28
Y34
Y36
Y40
Y8

OMIT_TABLE


U1100
LYNXPPOINT
MOBILE
FCBGA
(11 OF 11)
VSS

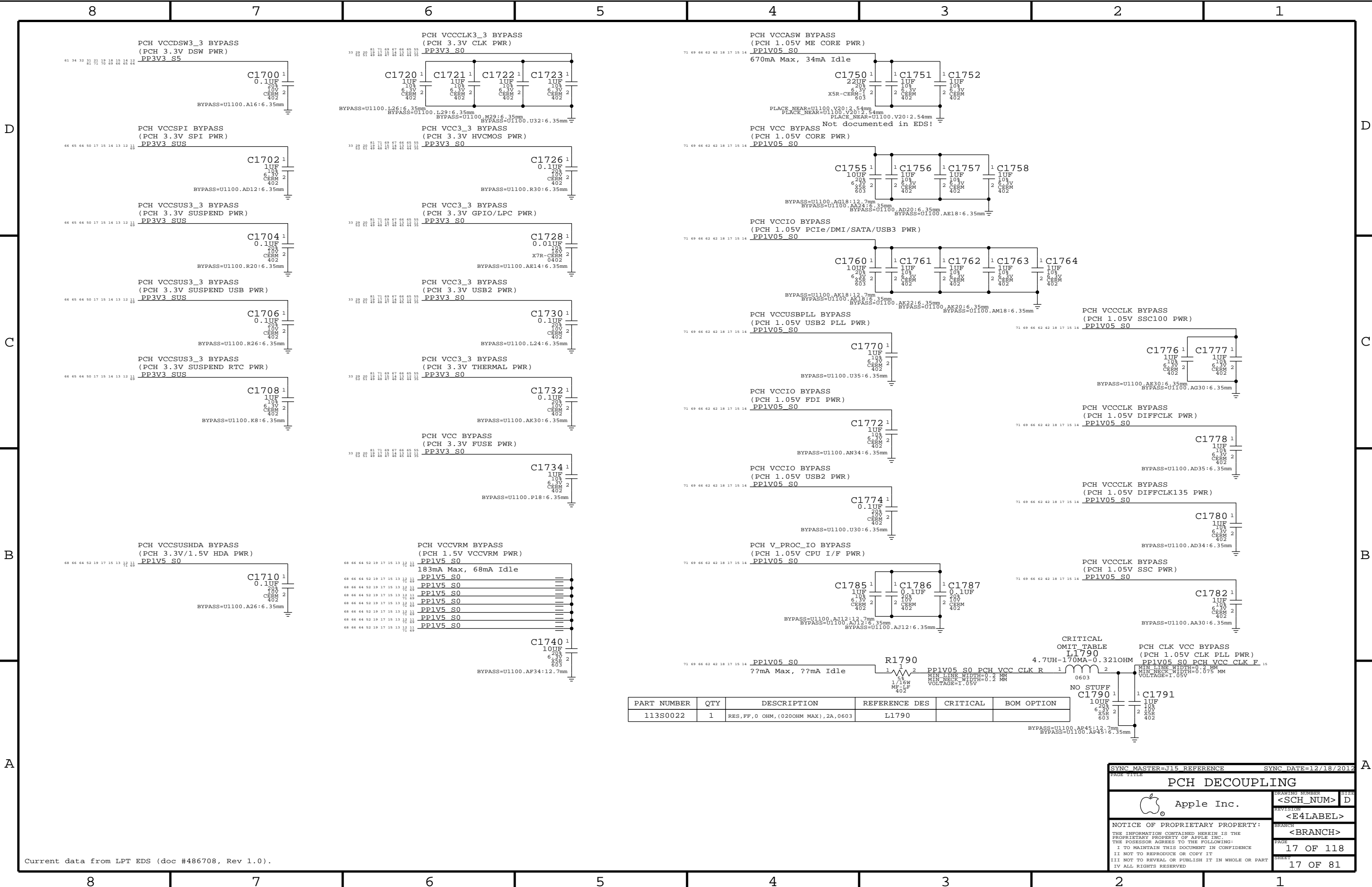
AA16
AA20
AA22
AA28
AA4
AB12
AB34
AB38
AB8
AC2
AC44
AD14
AD16
AD18
AD30
AD32
AD40
AD6
AD8
AE16
AE28
AF38
AF8
AG16
AG2
AG26
AG28
AG44
AJ16
AJ18
AJ20
AJ22
AJ24
AJ34
AJ38
AJ6
AJ8
AK14
AK24
AK43
AK45
AL12
AL2
BC22
BB42

VSS


VSS

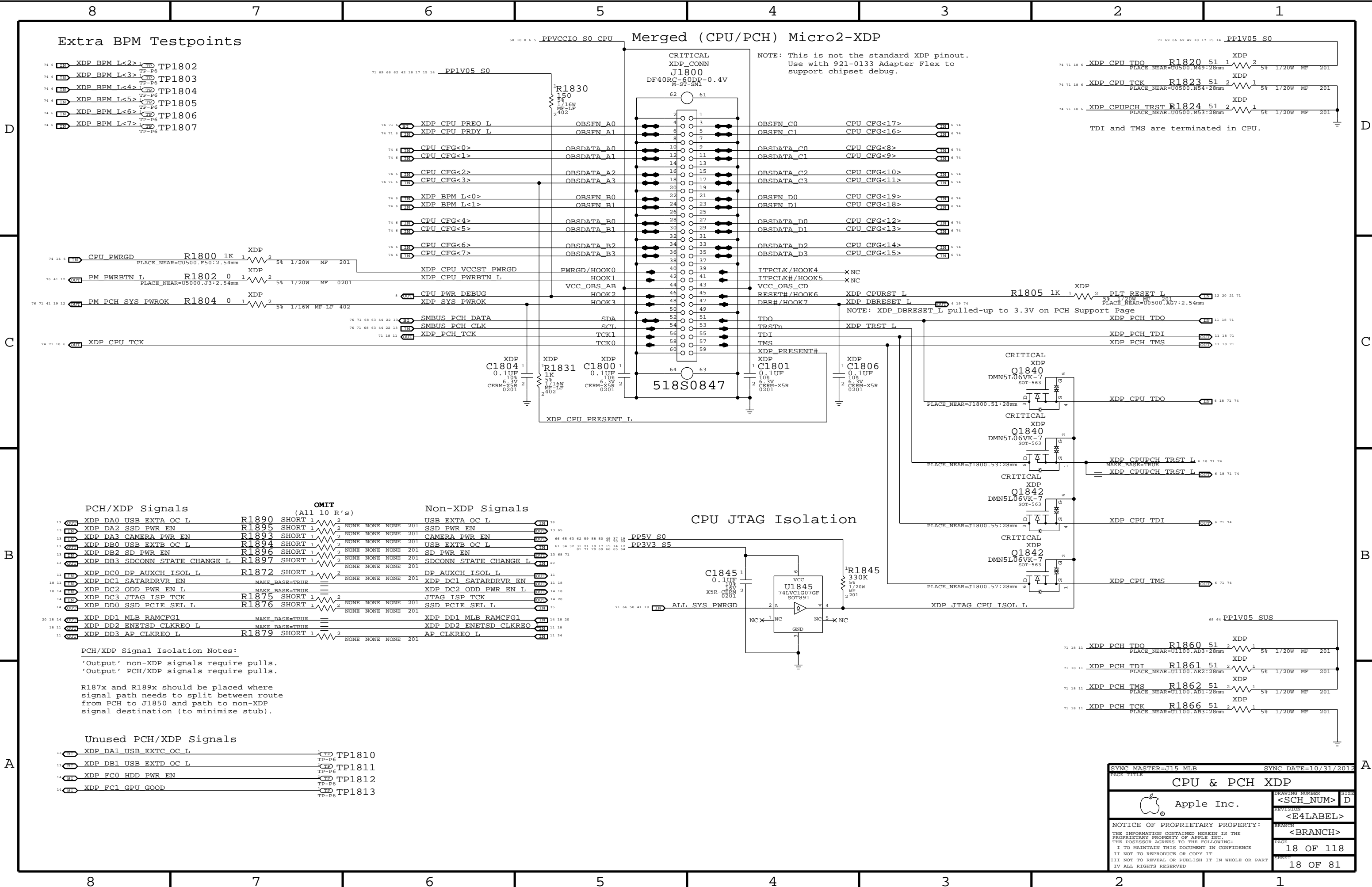
B19
B23
B27
B31
B35
B39
B7
BA40
BD11
BD15
BD19
AY36
AT43
BD31
BD35
BD39
BD7
D25
AV7
F15
F20
F29
F33
BC16
D4
G2
G38
G44
G8
H10
H13
H17
H22
H24
H26
H31
H36
H40
H7
K10
K15
K20
K29
K33
BC28

SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
PCH Grounds			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	16 OF 118
		SHEET	16 OF 81

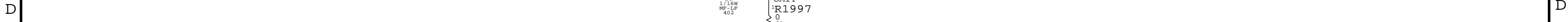


Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
PCH DECOUPLING			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	BRANCH
		<E4LABEL>	<BRANCH>
		PAGE	17 OF 118
		SHEET	17 OF 81

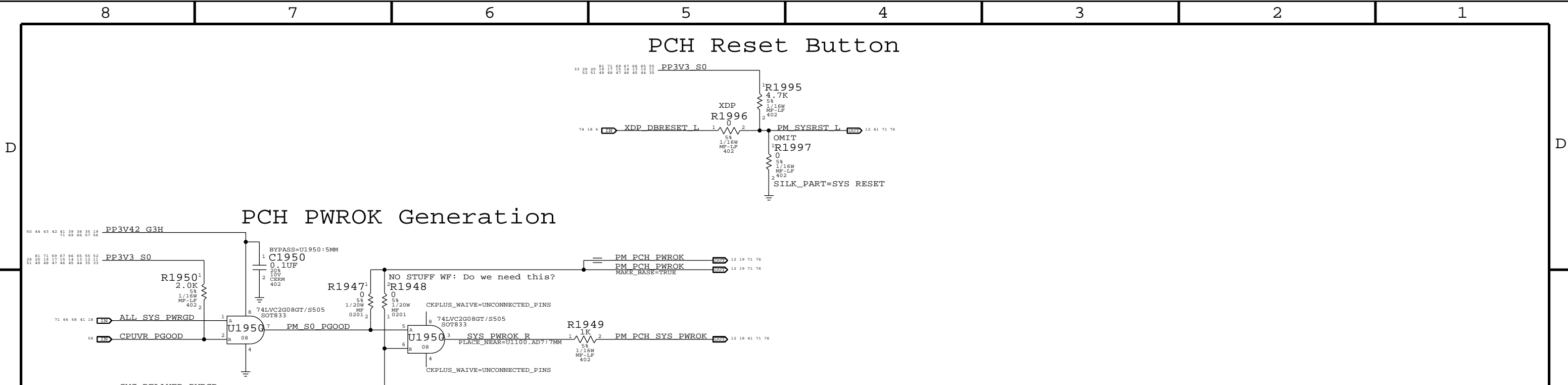


8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



42 41 30 29 **END** SMC_DELAYED_PWRGD

NOTE: ALL SMC_DELAYED_PWRGD must remain low until at



42 41 30 29 **END** SMC_DELAYED_PWRGD

NOTE: ALL SMC_DELAYED_PWRGD must remain low until at

B PCH ME Disable Strap B



VDDIO_25M_A: SB power rail for XTAL circuit.	96 98 44 43 42 41	37 36 35 34 33	PE3V42_G3H	UM2T (200 ohm ± 10% R20)	SMC controls strap enable to allow in-field control of strap setting.
VDDIO_25M_B: Camera power rail for XTAL circuit.					Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

GreenClk 25MHz Power

PP3V3 S5

Coin-Cell: 3.42V G3Hot: 3.42V G3Hot
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

PP5V S0

Q1920
DMN5L06VK.m7
SOT-563

SPI_DESCRIPTOR_OVERRIDE LS5V

R1920
100K
1/20W
2501

Timing diagram for SPI_DESCRIPTOR_OVERRIDE signal. The diagram shows a clock signal (SB XTAL Power) and a data signal (SPI_DESCRIPTOR_OVERRIDE). The data signal is high for a duration of 100 ns, then transitions to low. The transition occurs at approximately 100 ns after the start of the high pulse.

Camera XTAL Power
TBT XTAL Power

36 PF1V2 CAM_X1A0PCE1VDD
69 28 20 PF3V3 TBT1C

NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

C1924 0.1UF CERM 402
C1920 0.1UF CERM 402
C1922 0.1UF CERM 402
C1902 1UF XSR 402-1

U1900
SLG3NB148CV
TOPN
CRITICAL

VIOE_25M_A 32.768K
VIOE_25M_B

VBAT and +V3.3A are internally ORED to create VDD_RTC_OUT.
+V3.3A should be first available ~3.3V power to reduce VBAT draw.

SYSCLK_CLK32K_RTC

Q1920
DMN5L06VK-7
SOT-563

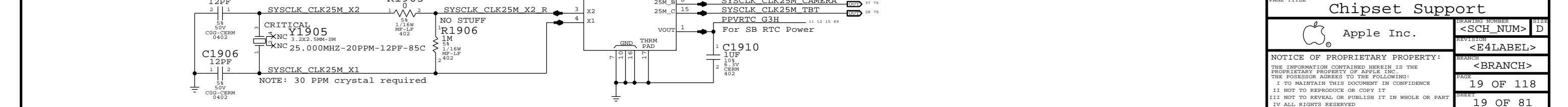
R1921
1K
1/20W
5%
201

HDA_SDOUT_R

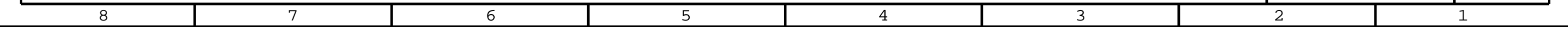
IPD = 9-50k

SPI_DESCRIPTOR_OVERRIDE_L

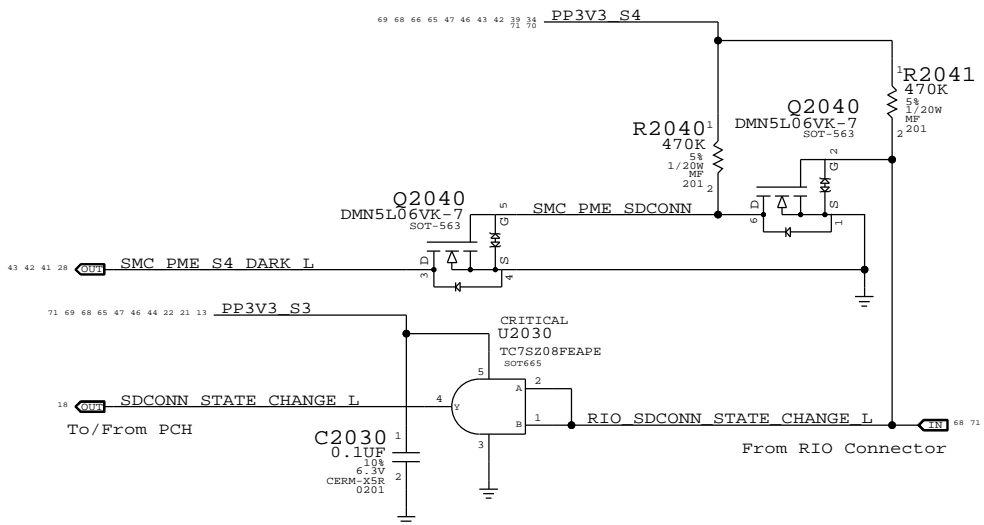
Timing diagram showing signals VIOE_25M_B, VIOE_25M_C, 25M_A, and SYSCLK_CLK25M_SB. The diagram includes a vertical dashed line indicating a specific time point. A table at the bottom right shows SYNC_MASTER=J15_REFERENCE and SYNC_DATE=12/18/2012.



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

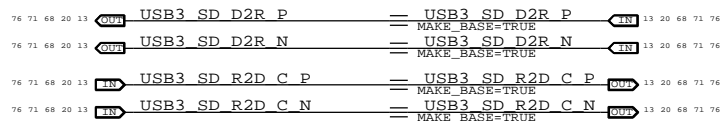


RIO SD Card Reader Support



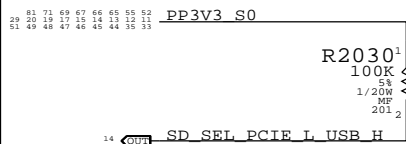
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.

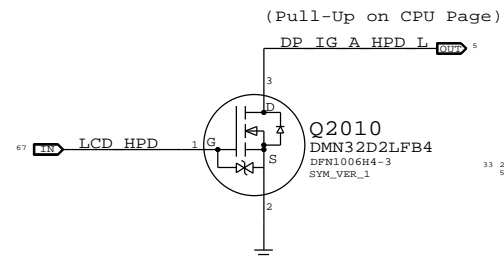


Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe



LCD HPD Inverter

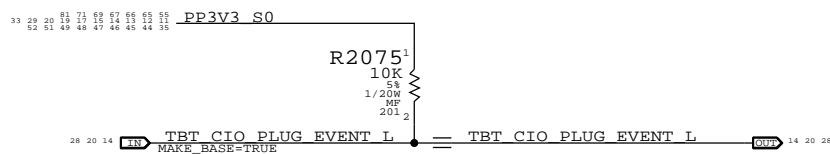


HDMI HPD pull-down



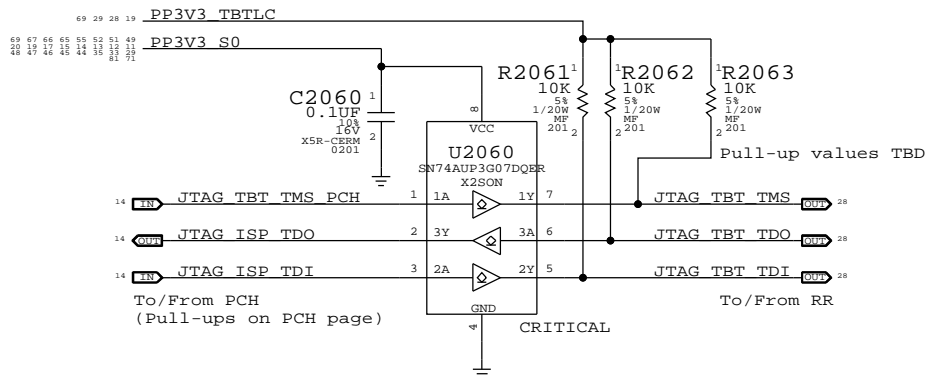
Redwood Ridge Support

RR output is open-drain, no isolation necessary

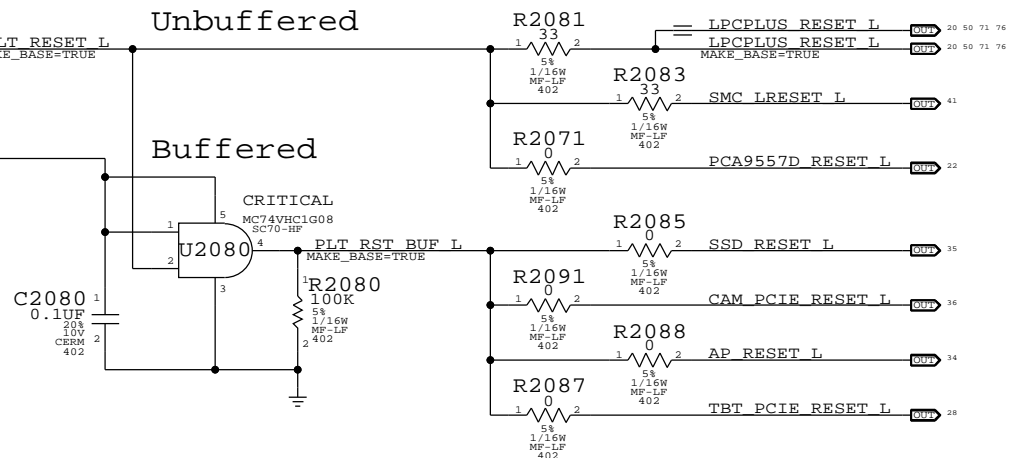


Redwood Ridge JTAG Isolation

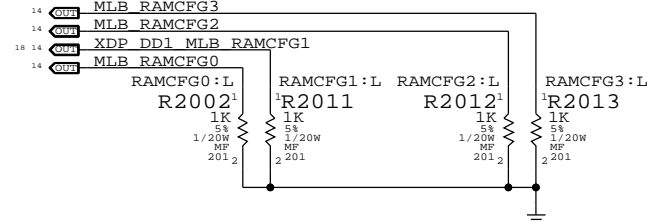
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



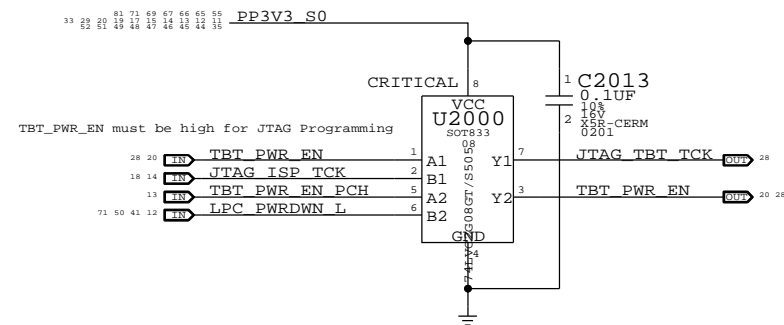
Platform Reset Connections



RAM Configuration Straps

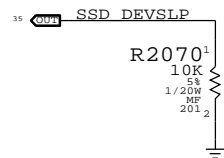


GPIO Glitch Prevention



GS3 Connector Support

DEVSLP not supported on LPT-H



SYNC MASTER=J15 REFERENCE		SYNC DATE=01/14/2013	
PAGE TITLE		Project Chipset Support	
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	20 OF 118
		SHEET	20 OF 81


D

D

C

A

A

SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
CPU Memory S3		Support	
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	
		21 OF 118	
		SHEET	
		21 OF 81	

C



A

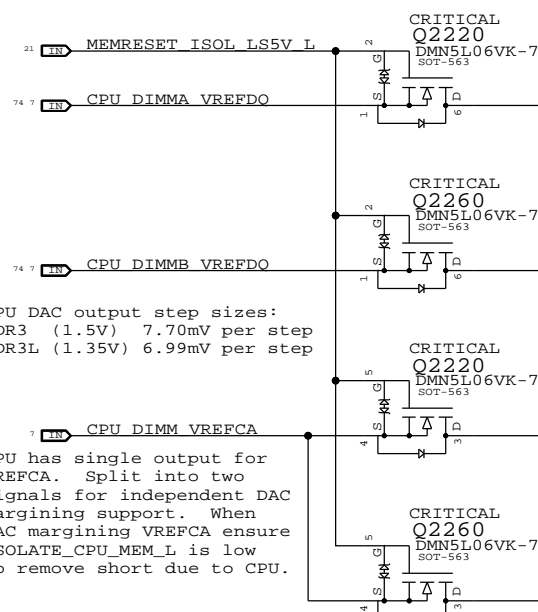
[illegible]

```
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFFDACS_SCL
- =I2C_VREFFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.
```

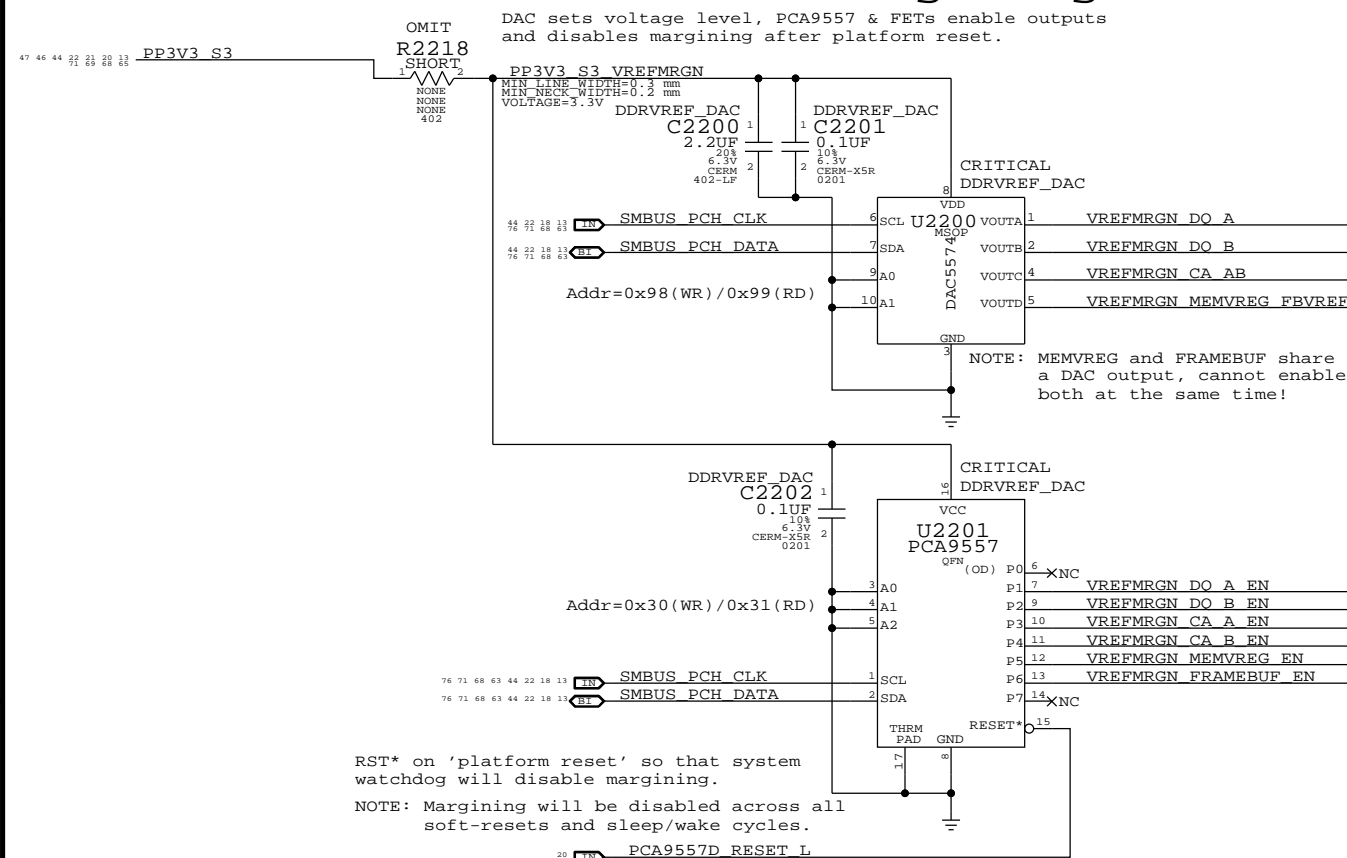
FETs for CPU isolation during S3



NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFOCA. Split into two signals for independent DAC margining support. When DAC margining VREFOCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

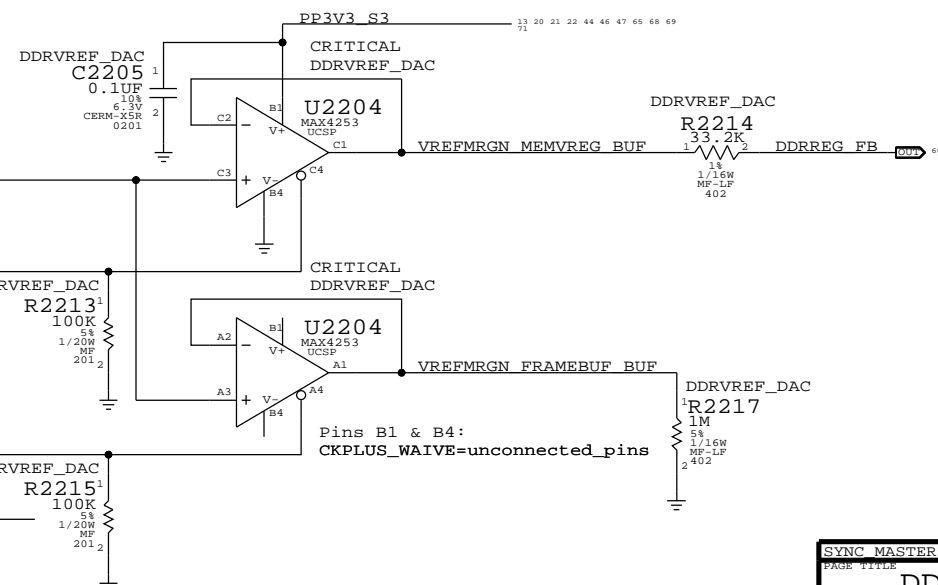
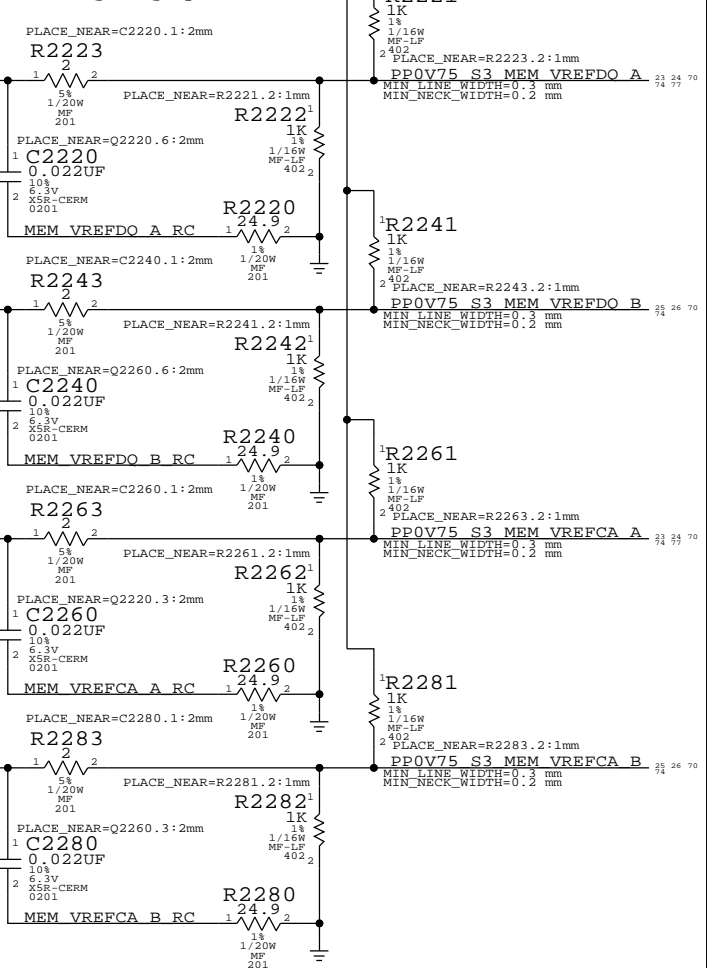



RST* on 'platform reset' so that system watchdog will disable margining.

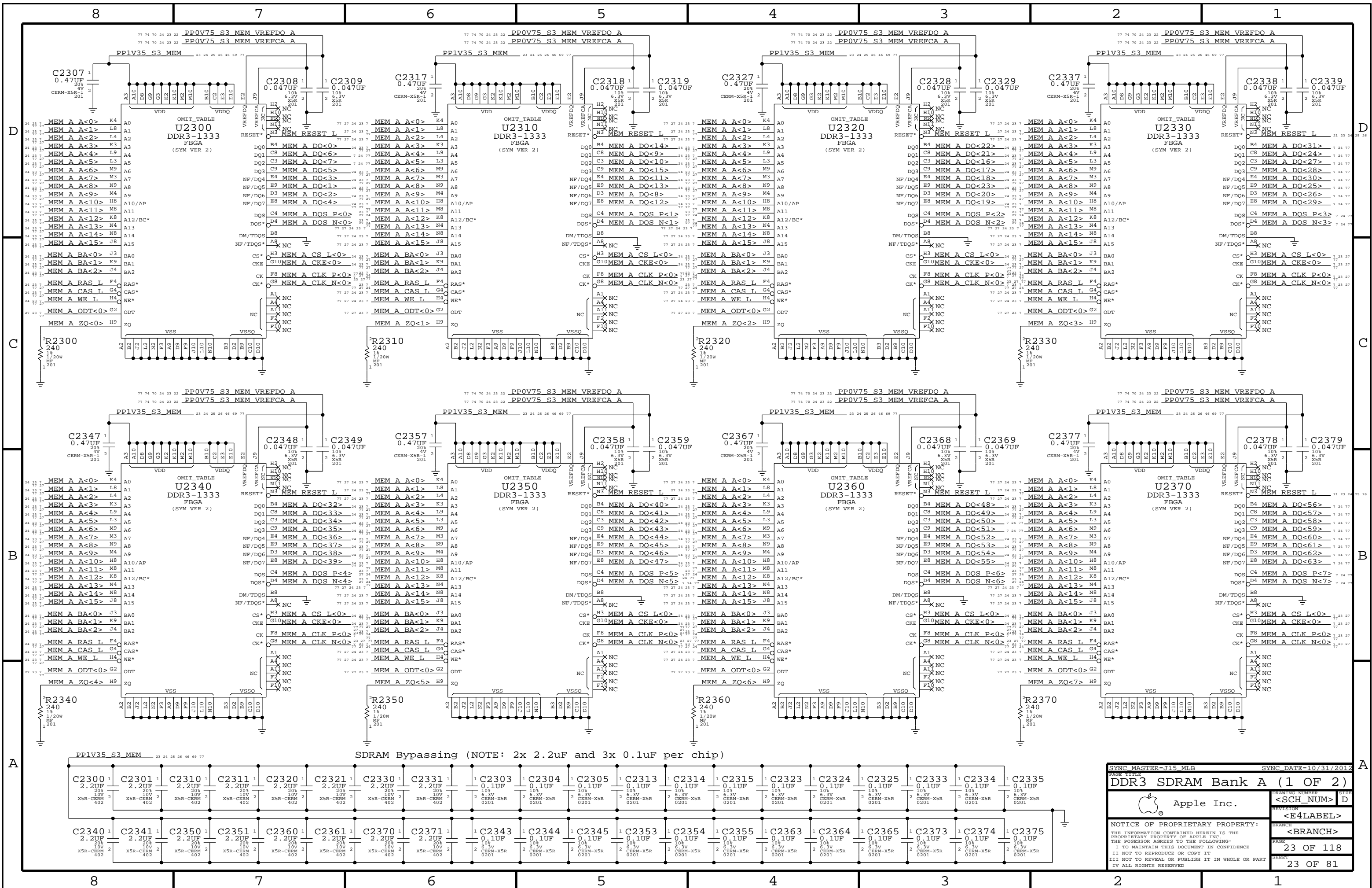
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
Vref current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

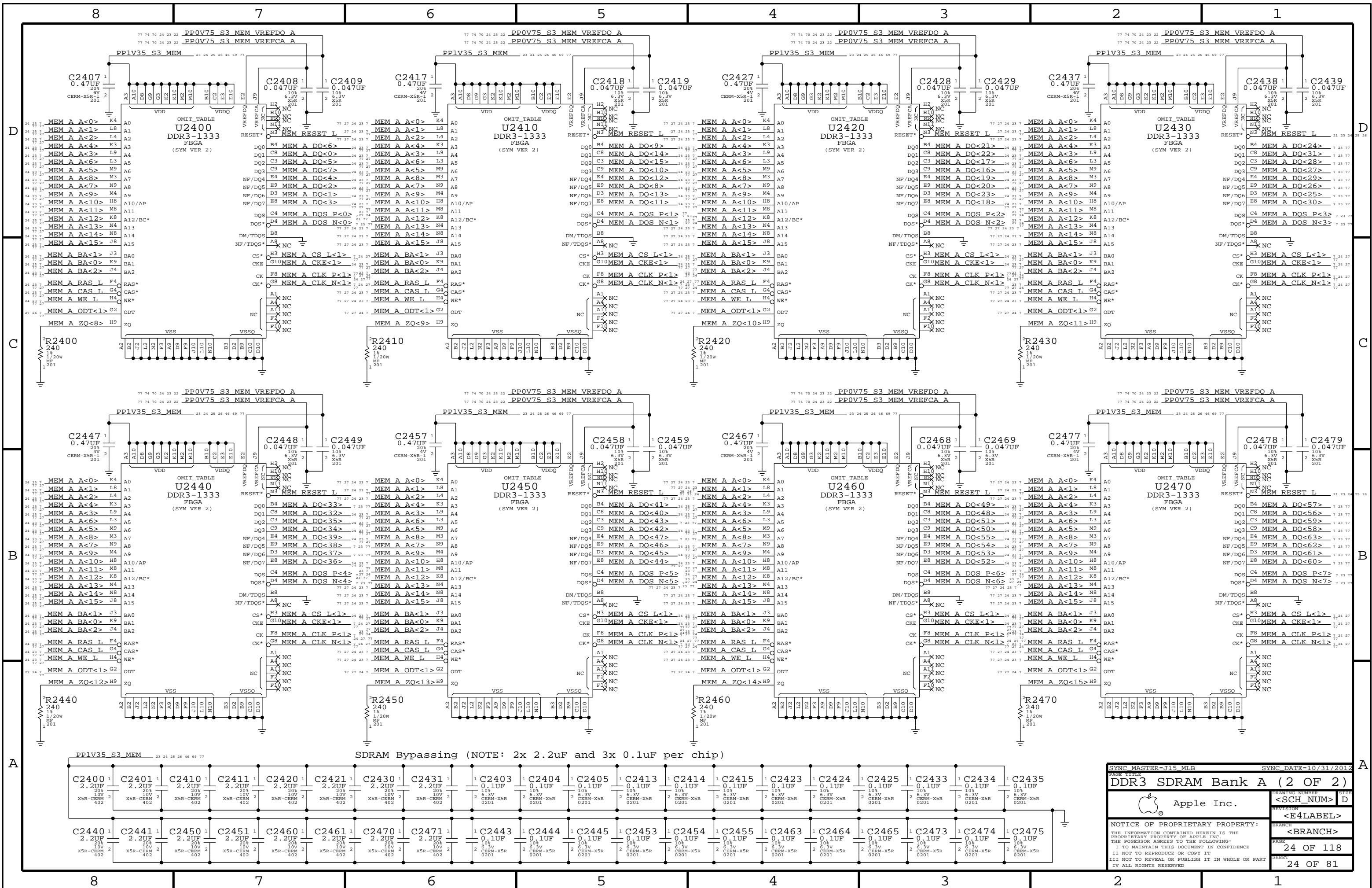
Always used, regardless
of margining option.



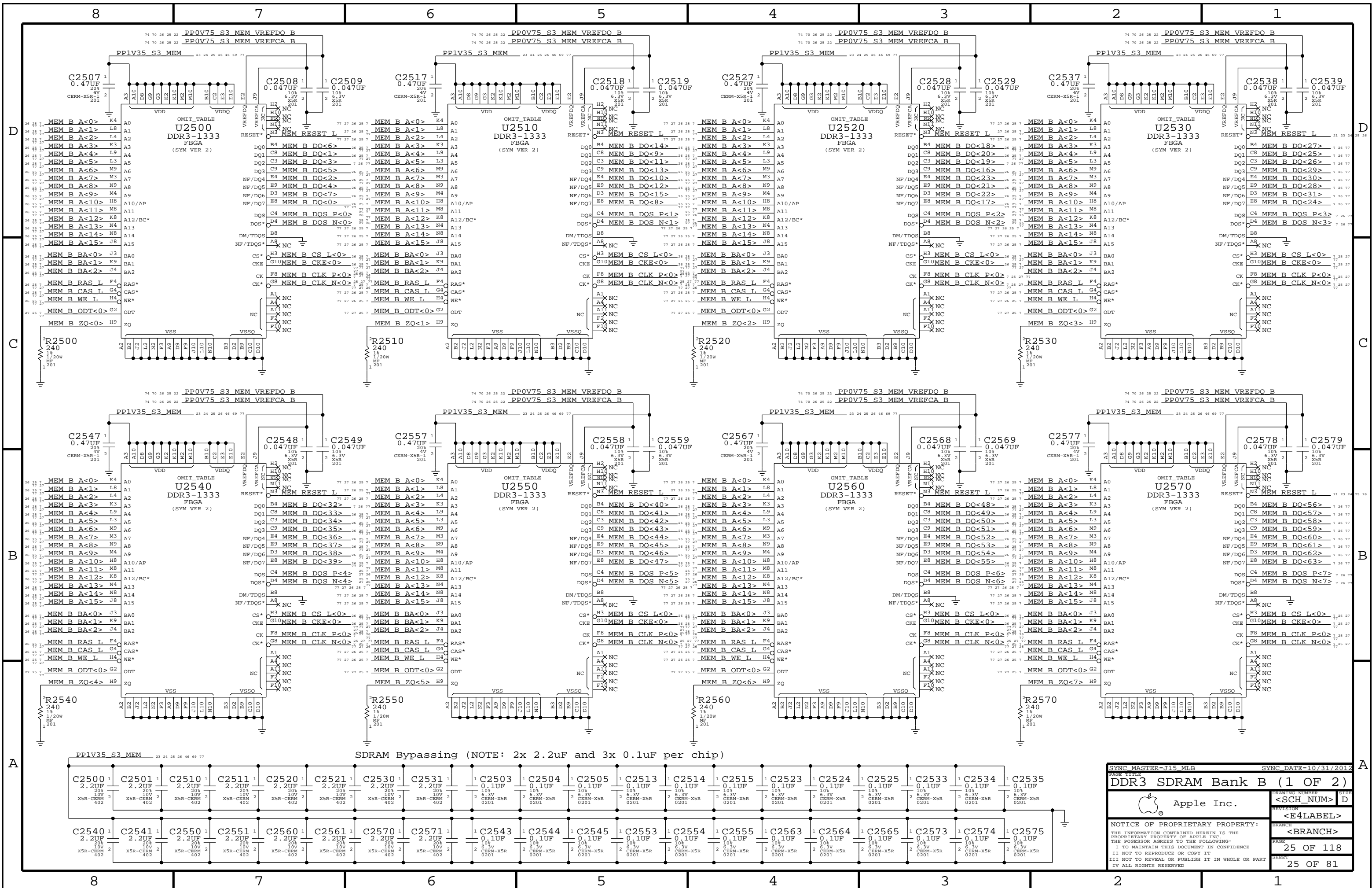
SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE			
DDR3 VREF MARGINING			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
		REVISION <E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I WILL NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		BRANCH <BRANCH> PAGE 22 OF 118 SHEET 22 OF 81	



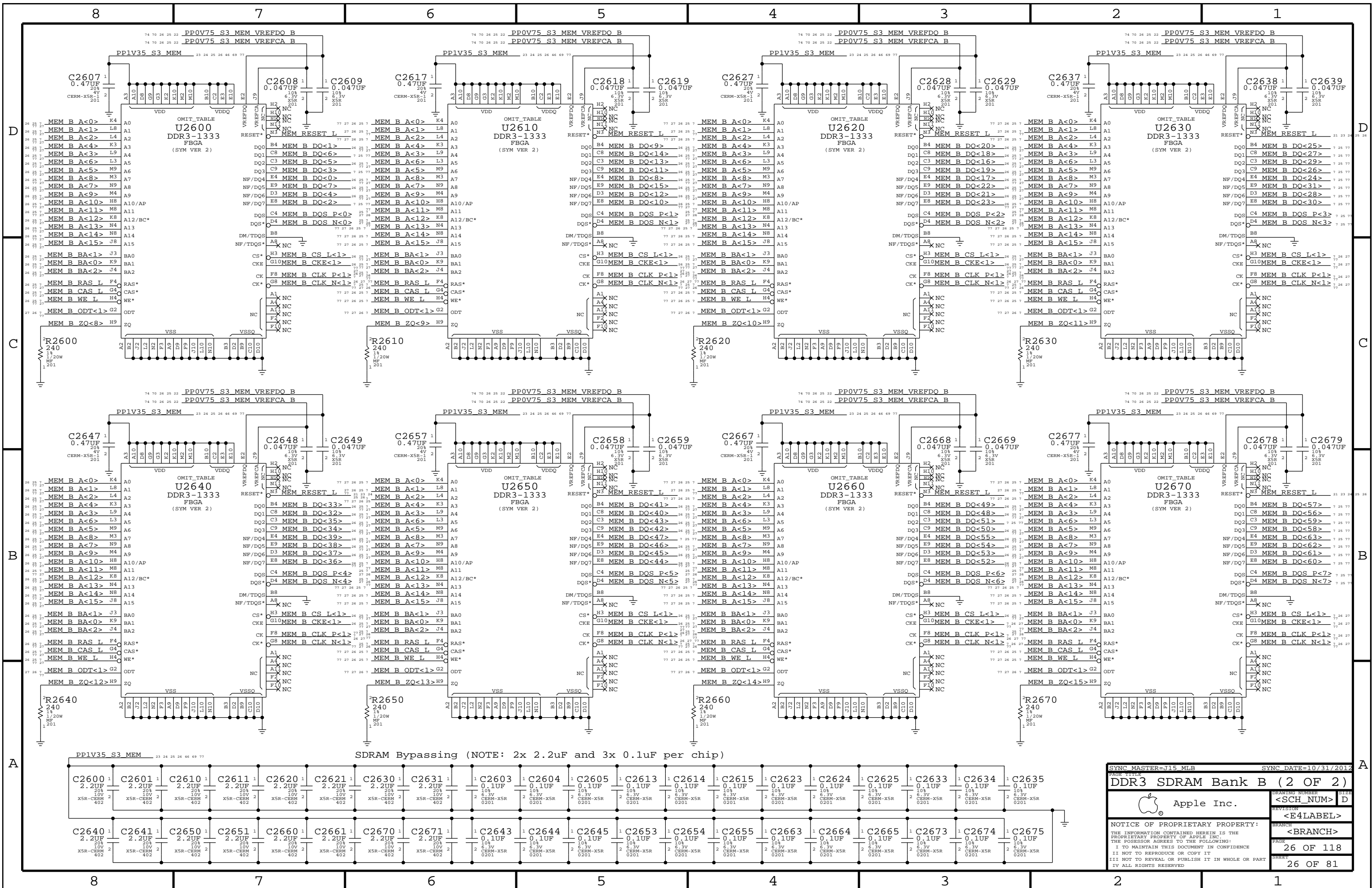
SYNC MASTER=J15 MLB
PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)
DRAWING NUMBER
<SCH_NUM>
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
23 OF 118
SHEET
23 OF 81
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
I NOT TO REPRODUCE OR COPY IT
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=J15 MLB
PAGE TITLE
DDR3 SDRAM Bank A (2 OF 2)
Apple Inc.
DRAWING NUMBER
<SCH NUM>
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
24 OF 118
SHEET
24 OF 81
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=J15 MLB
PAGE TITLE
DDR3 SDRAM Bank B (1 OF 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
25 OF 118
SHEET
25 OF 81
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE

DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH NUM> D

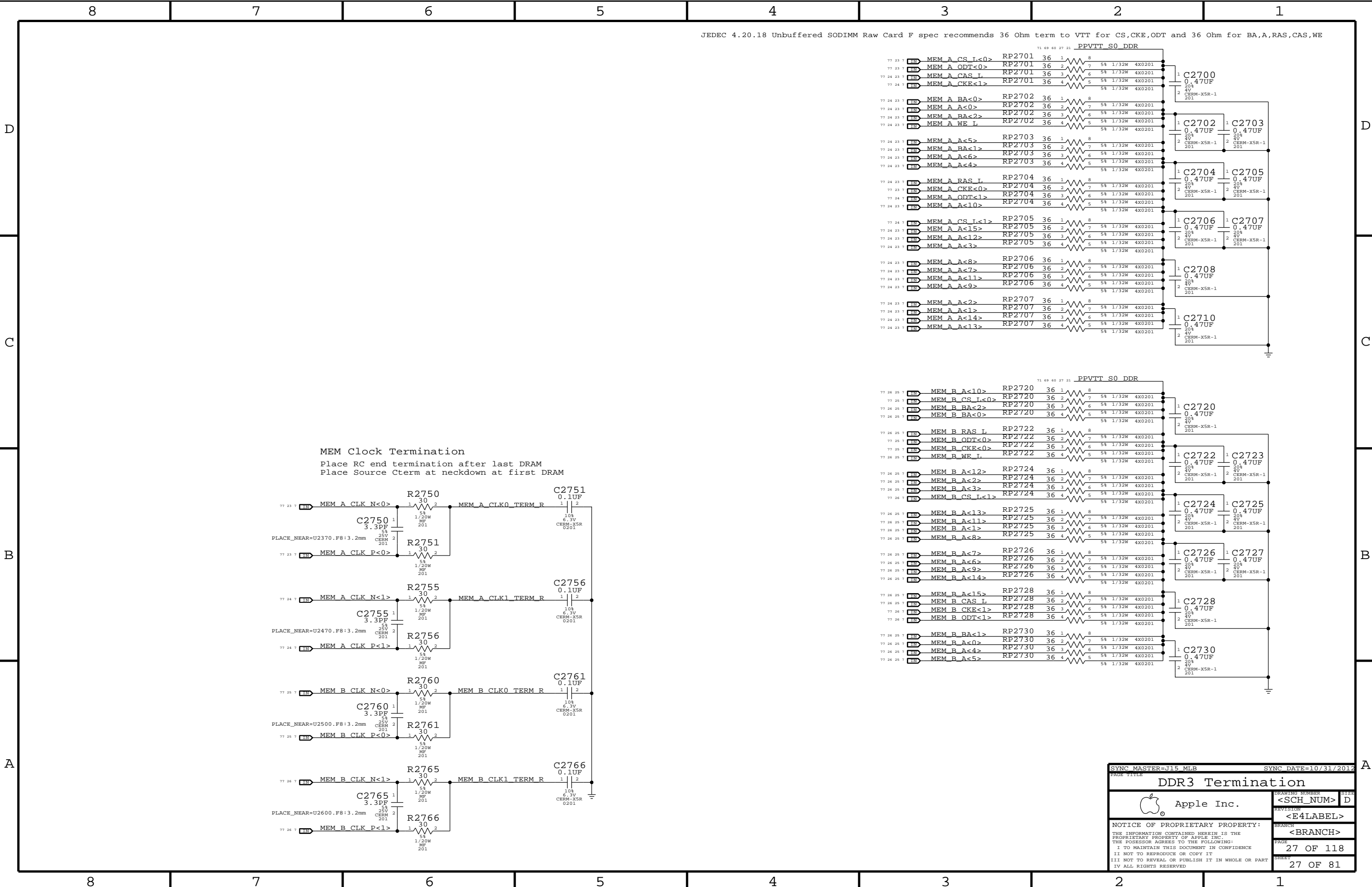
REVISION <E4LABEL>

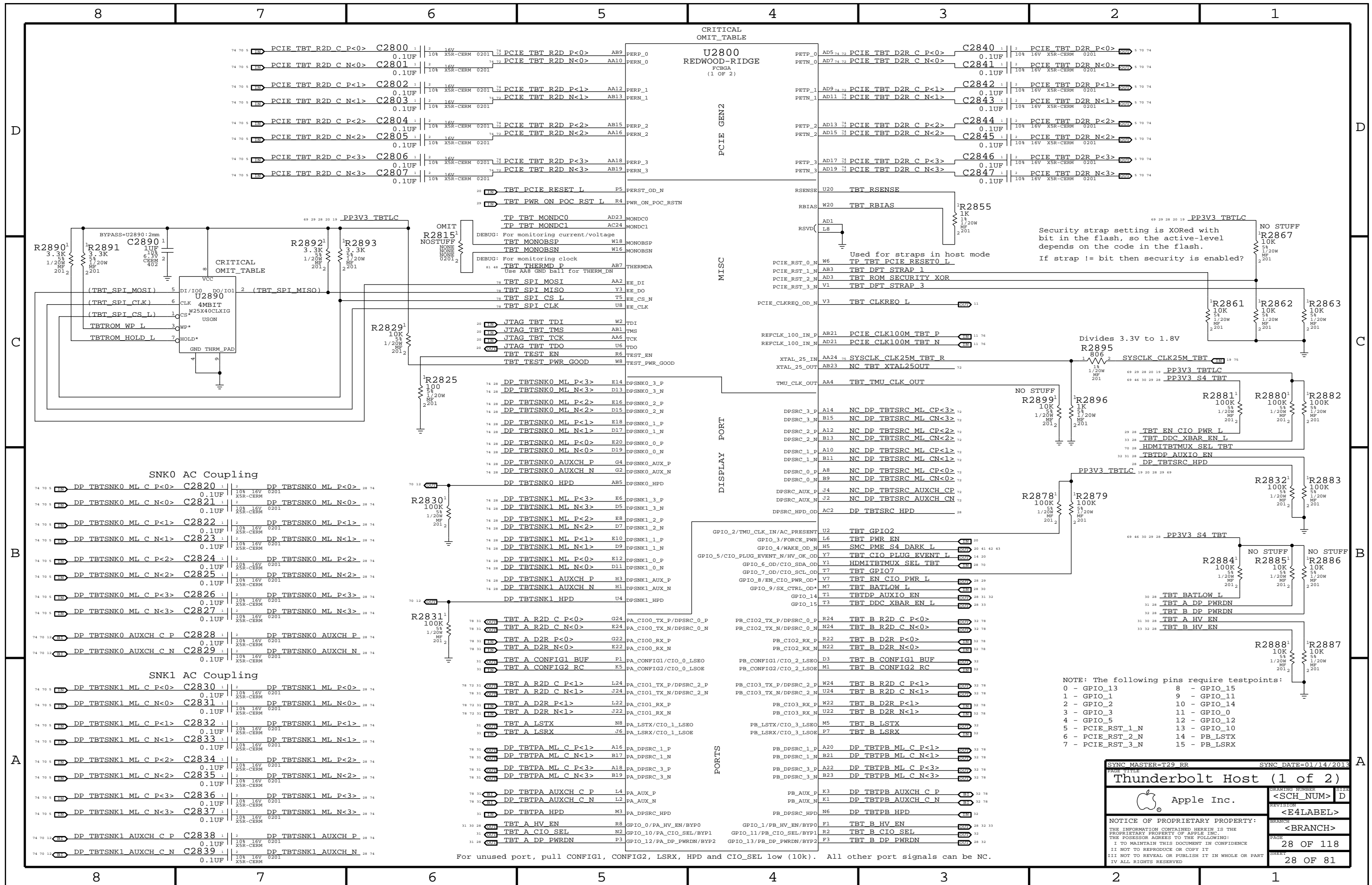
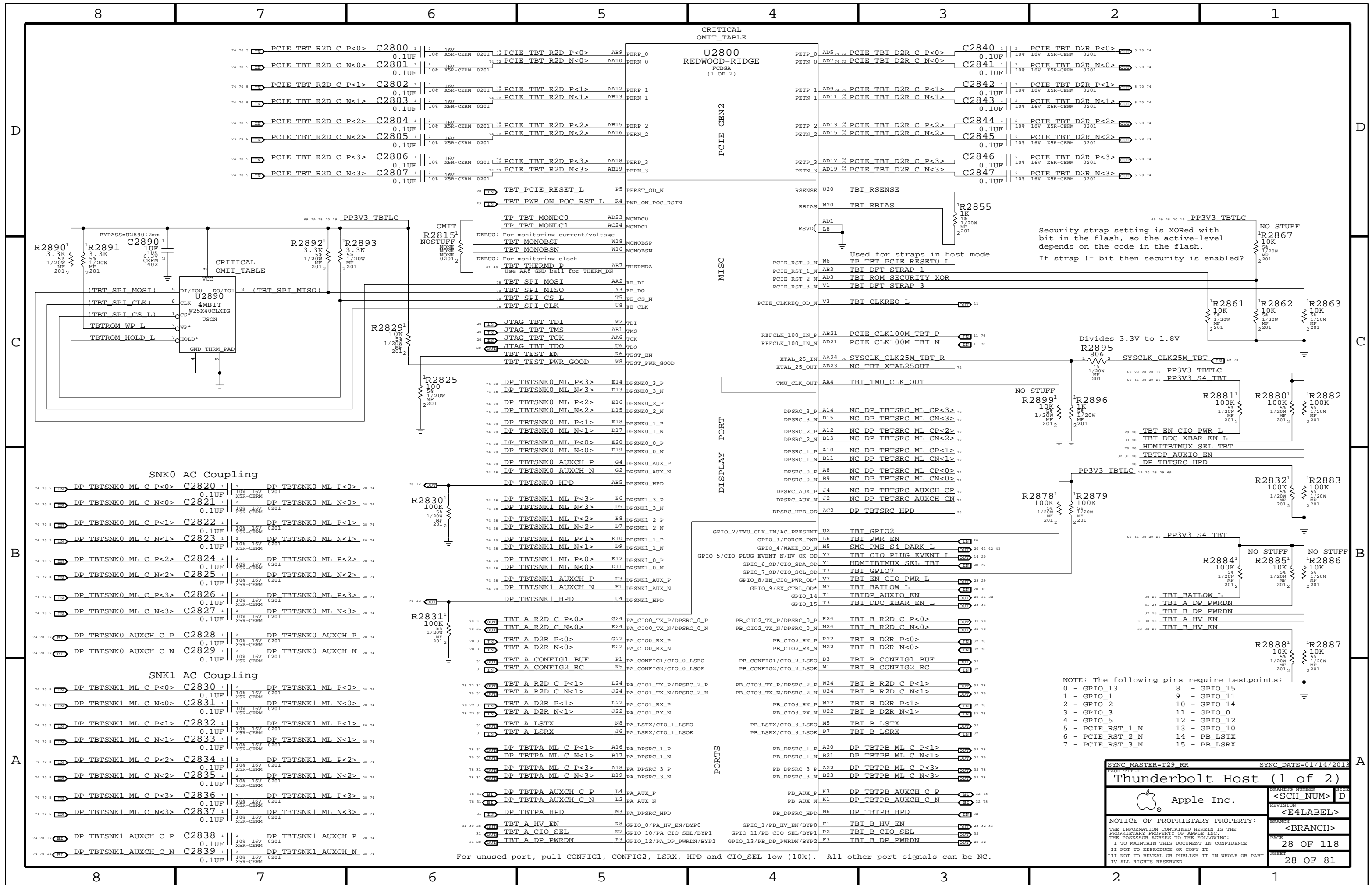
BRANCH <BRANCH>

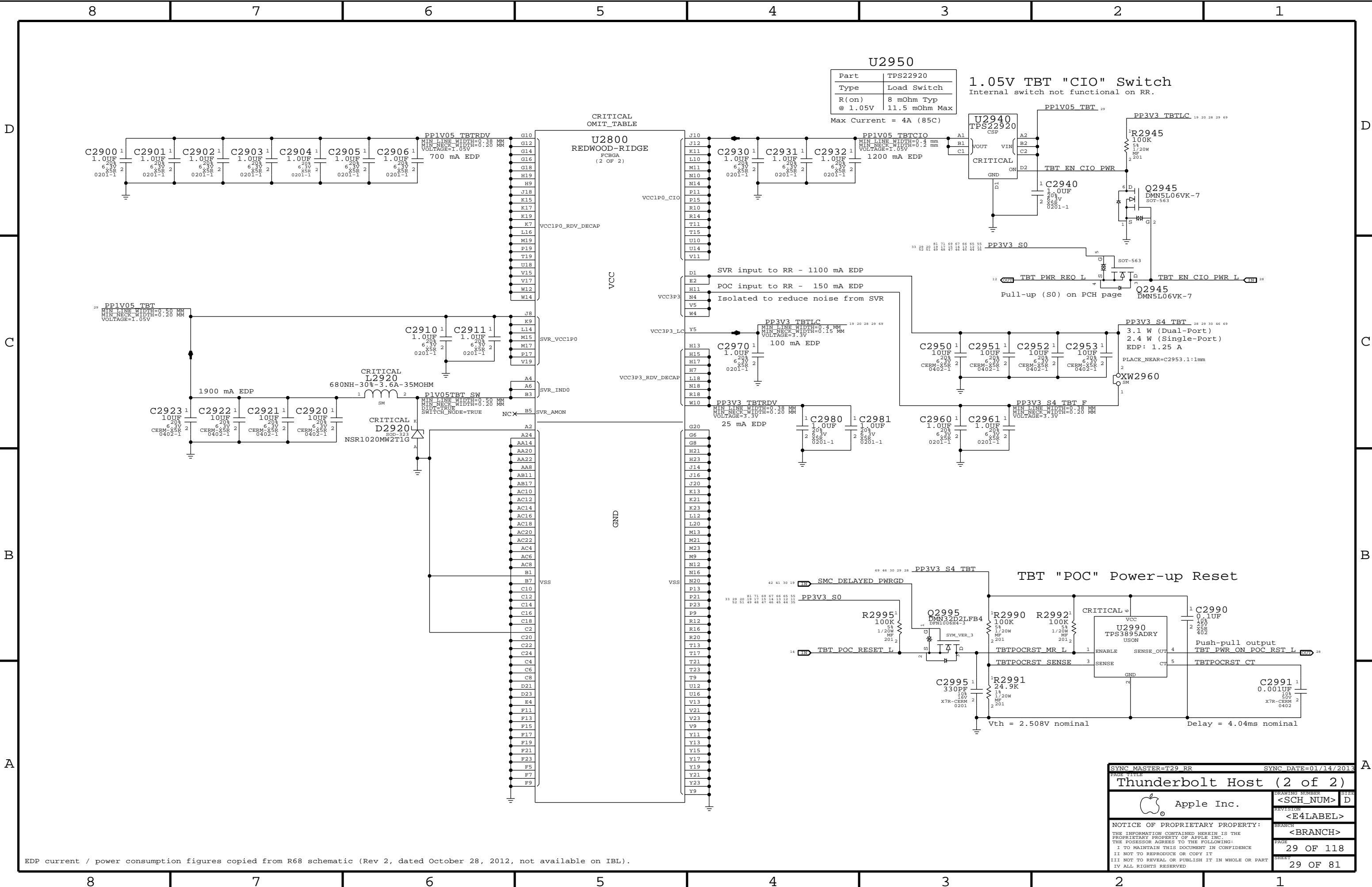
PAGE 26 OF 118

SHEET 26 OF 81

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED








EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max
Max Current = 4A (85C)	

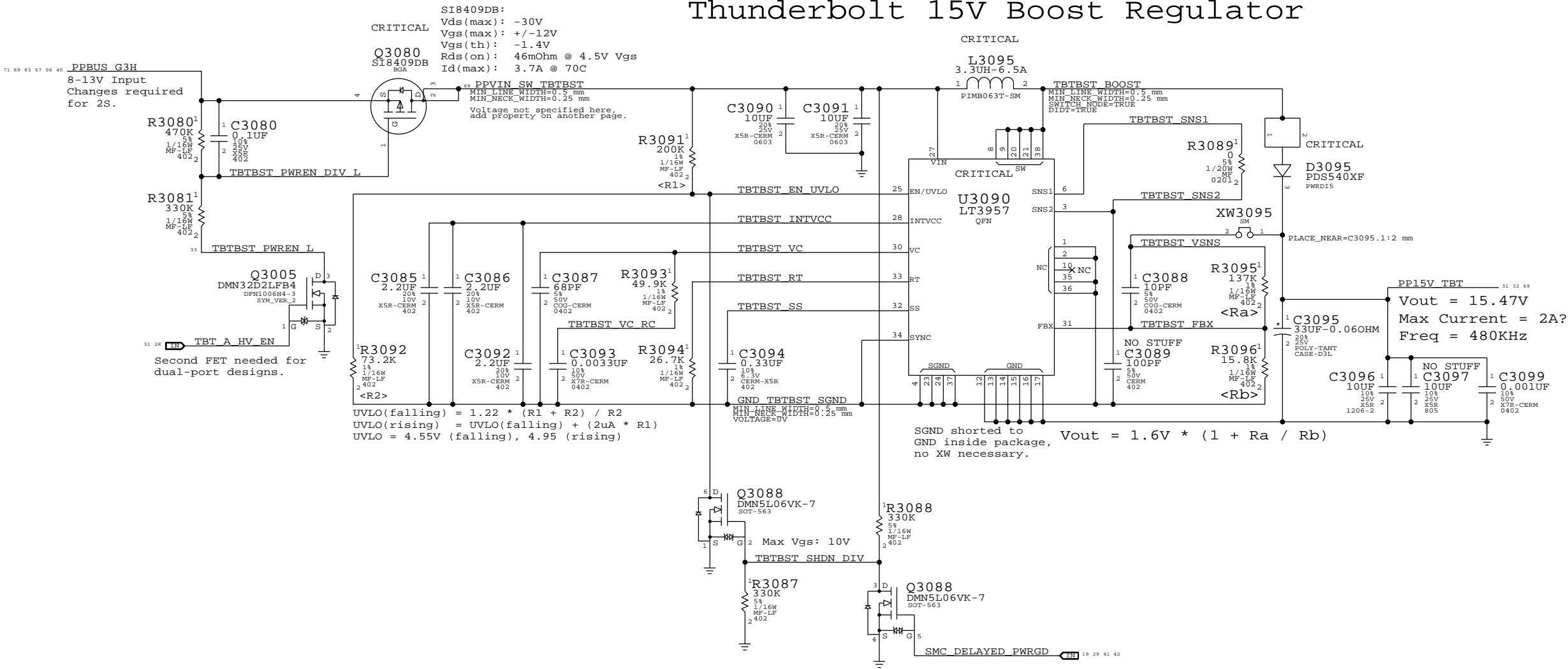
1.05V TBT "CIO" Switch
Internal switch not functional on RR.

SYNC MASTER=T29 RR		SYNC DATE=01/14/2013	
PAGE TITLE		Thunderbolt Host (2 of 2)	
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	BRANCH
		<E4LABEL>	<BRANCH>
		PAGE	29 OF 118
		SHEET	29 OF 81

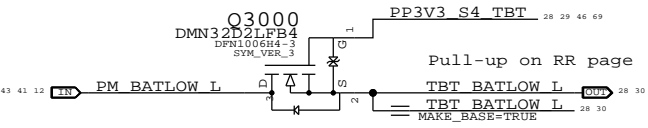
Page Notes


Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



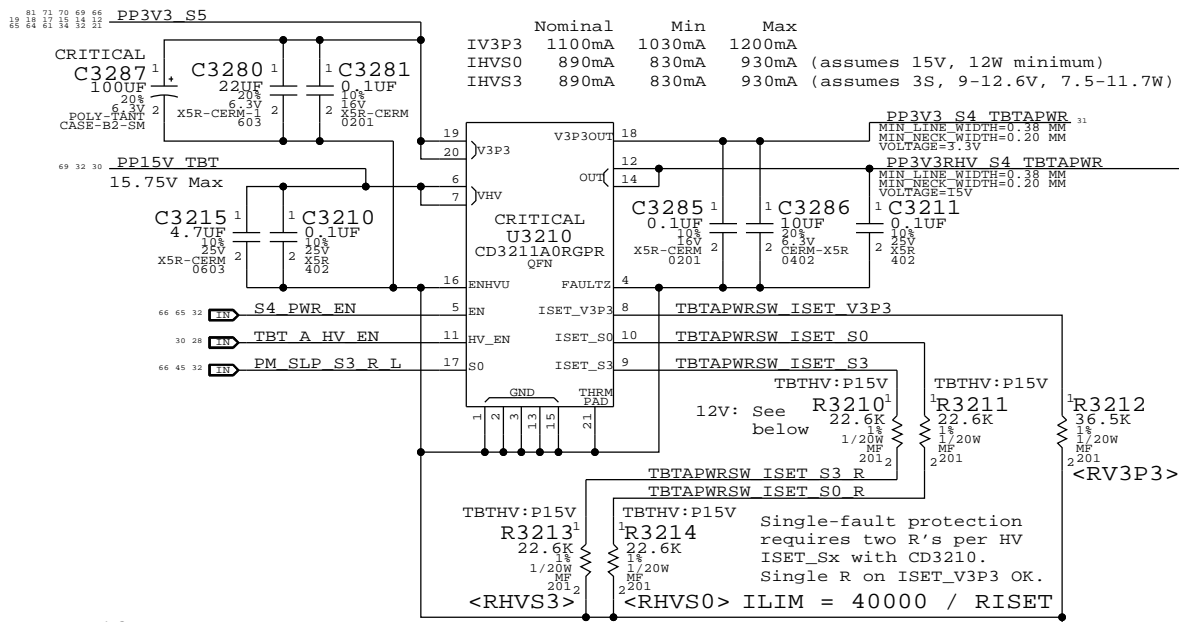
BATLOW# Isolation



SYNC MASTER=T29 RR		SYNC DATE=01/14/2013	
PAGE TITLE			
Thunderbolt Mobile Support			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		<BRANCH>	
		PAGE	30 OF 118
		SHEET	30 OF 81

3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

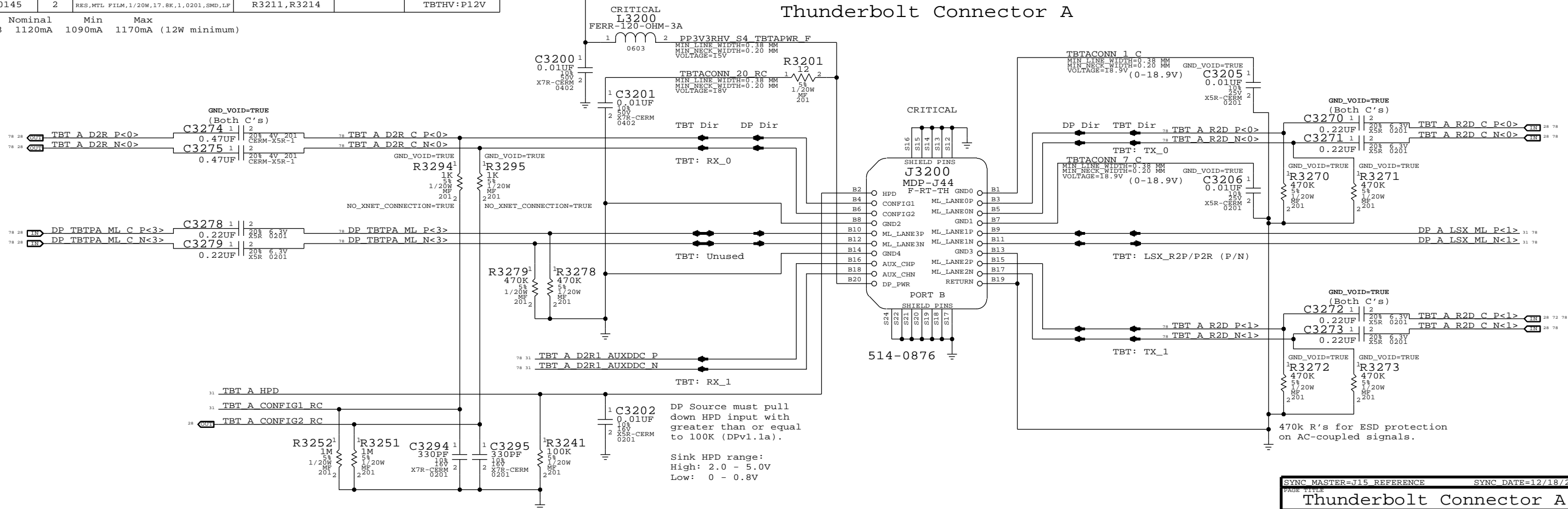



For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

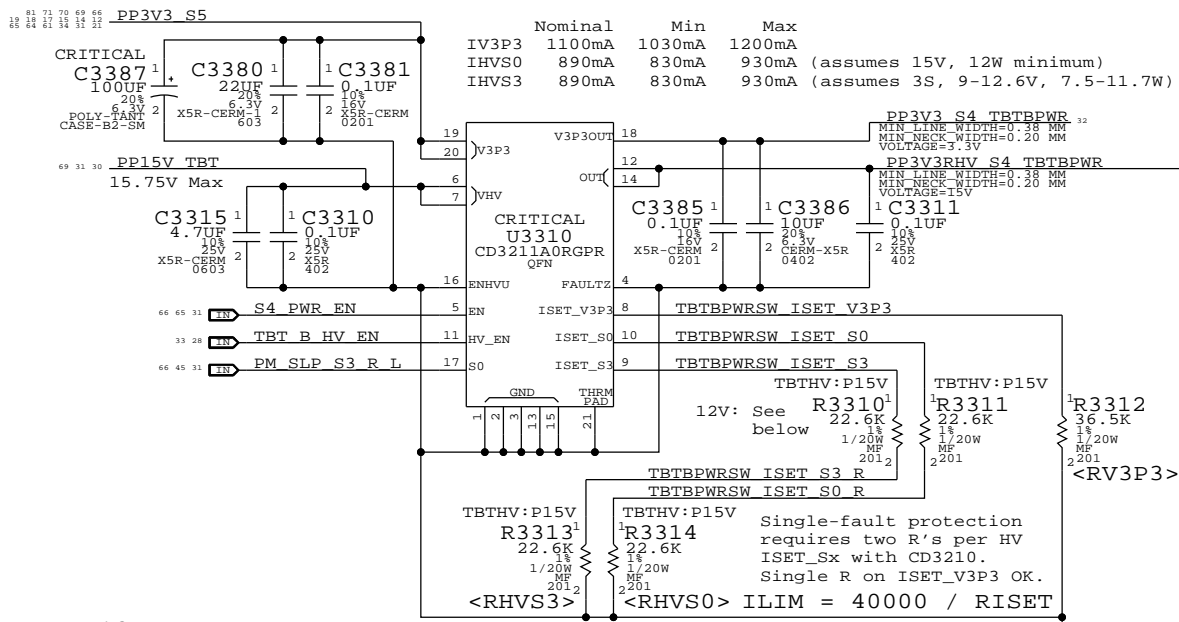
Thunderbolt Connector A



SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
Thunderbolt Connector A			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE IT NOT TO REPRODUCE OR COPY IT I/I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I/V ALL RIGHTS RESERVED		<BRANCH>	
		PAGE	32 OF 118
		SHEET	31 OF 81

3.3V/HV Power MUX

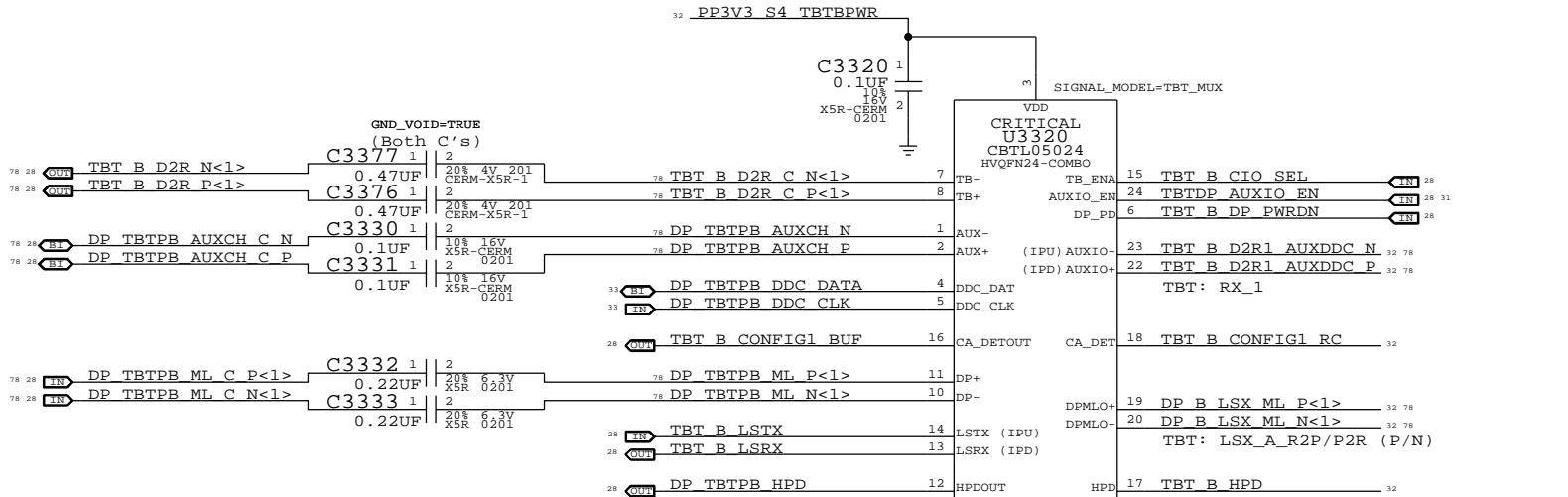
V3P3 must be S4 to support wake from Thunderbolt devices.



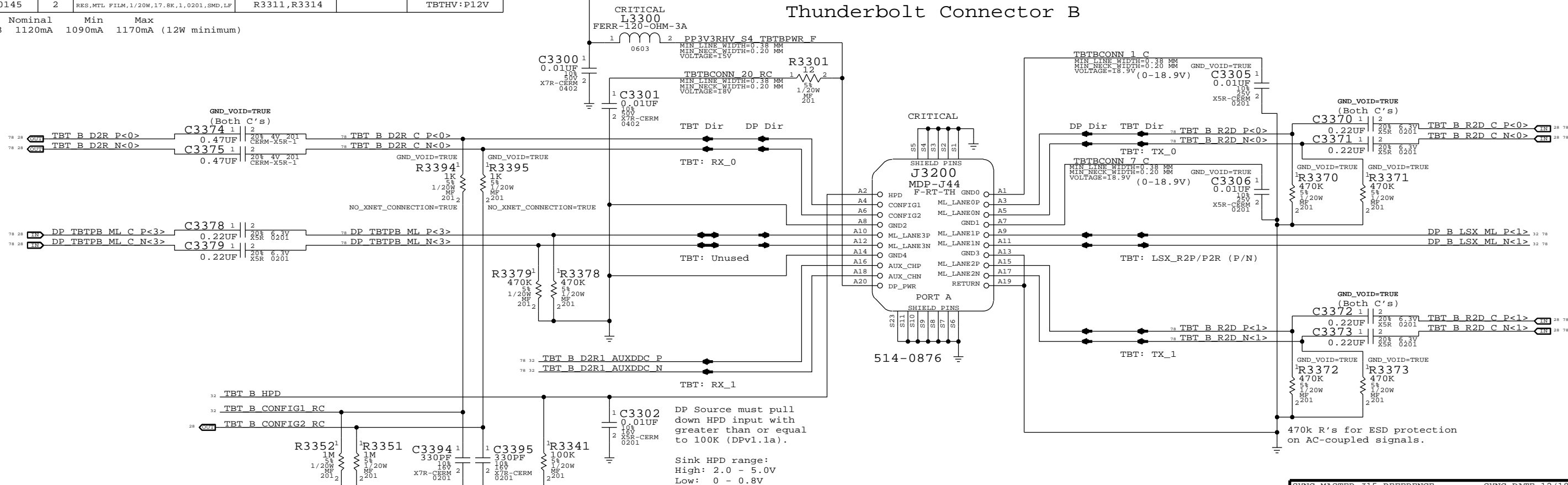
For 12V systems:


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

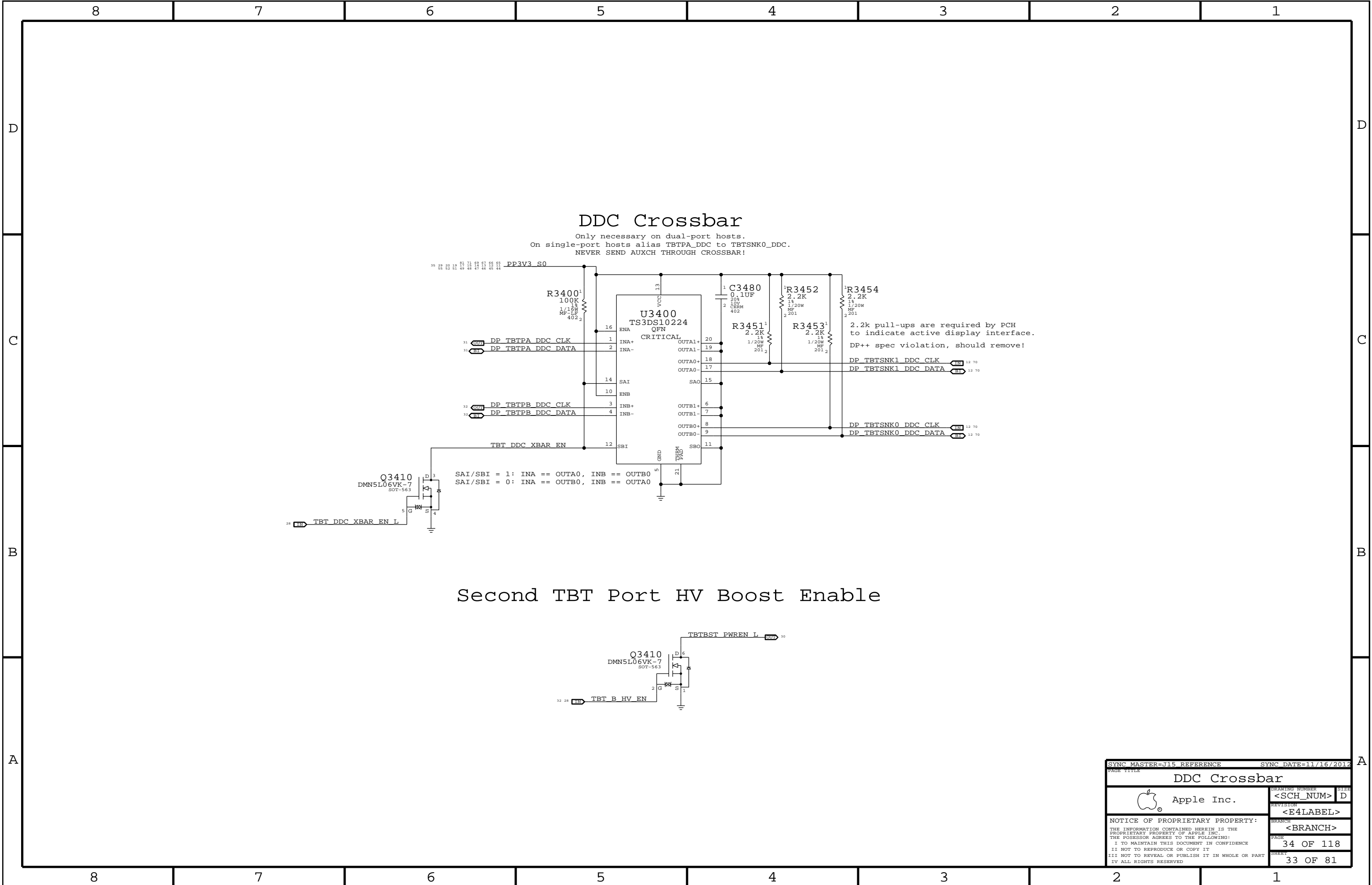
Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

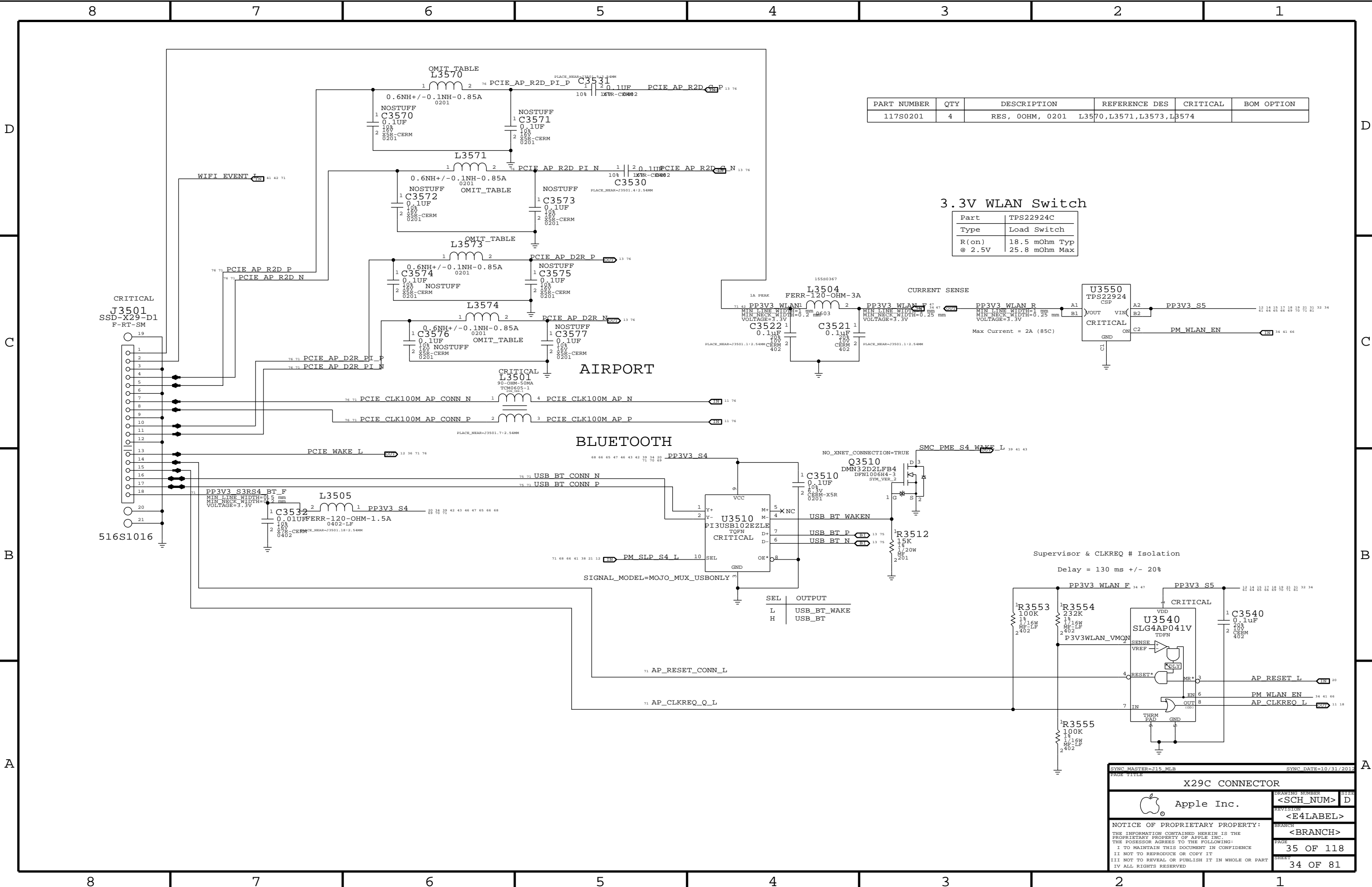


Thunderbolt Connector B



SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
Thunderbolt Connector B			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		<BRANCH>	
		PAGE	33 OF 118
		SHEET	32 OF 81






PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 00HM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE			
X29C CONNECTOR			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	
		<E4LABEL>	
		BRANCH	<BRANCH>
		PAGE	35 OF 118
		SHEET	34 OF 81

D

C

B

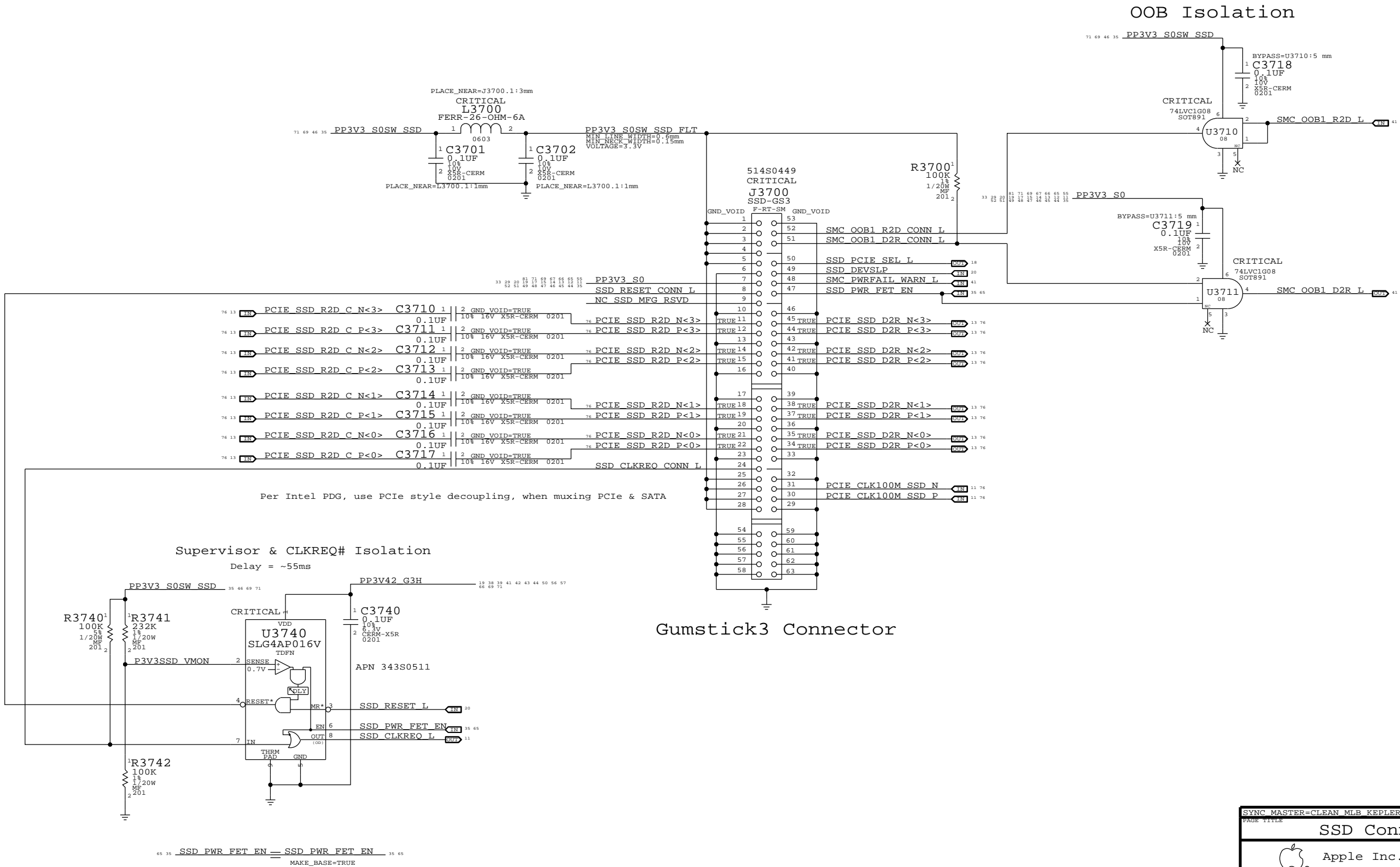
A


D

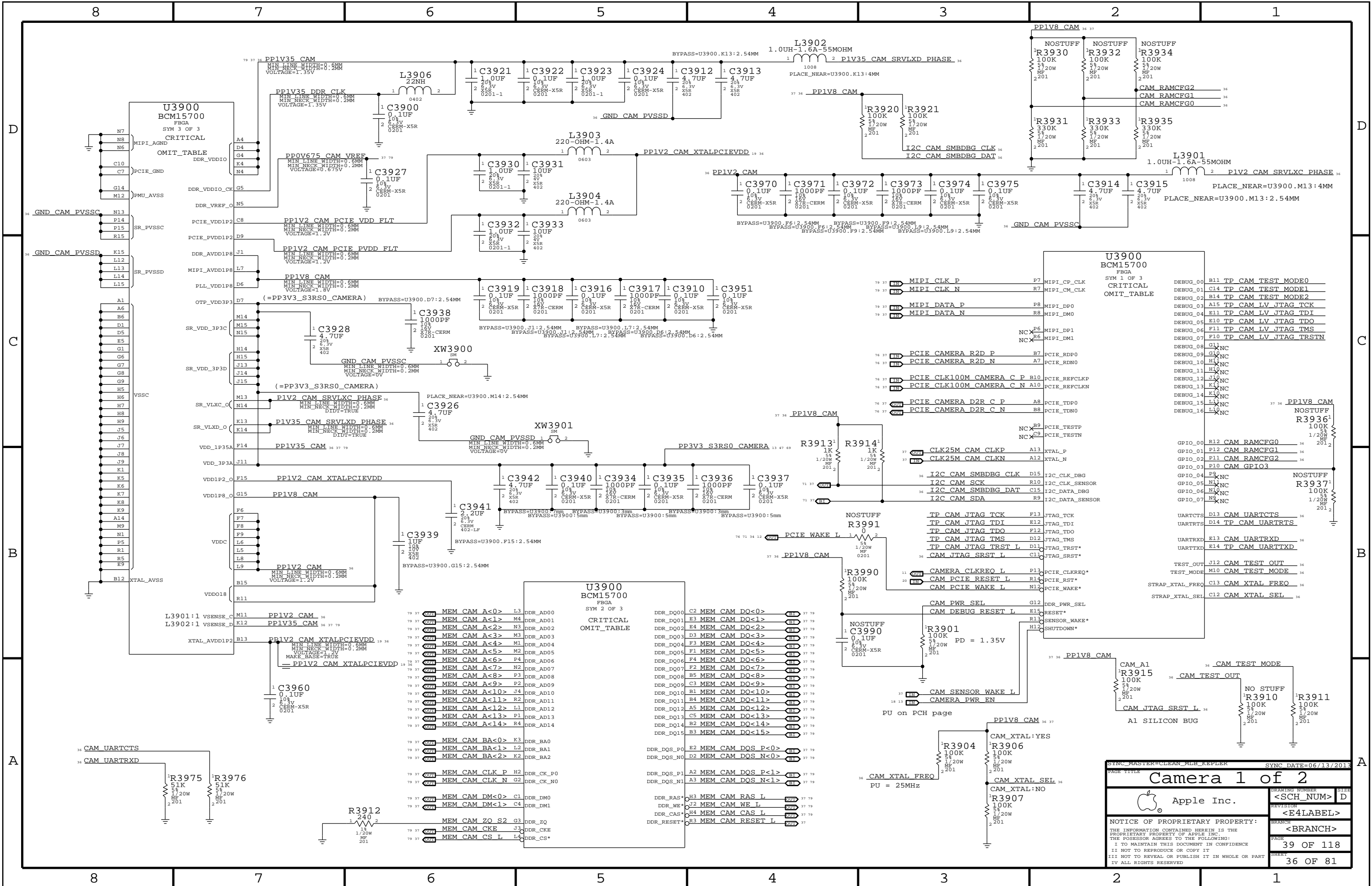
C

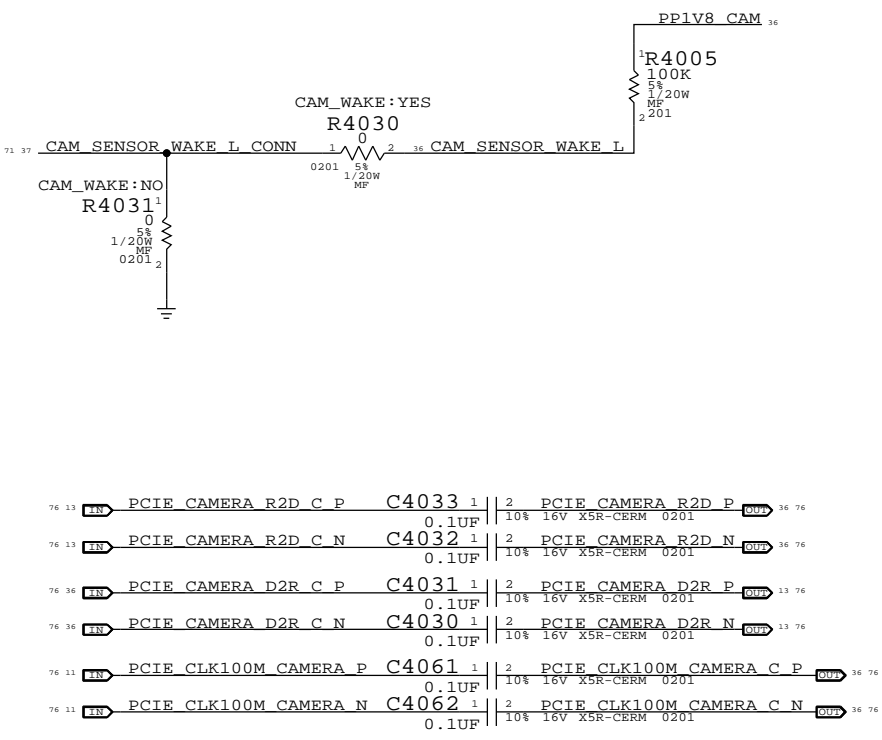
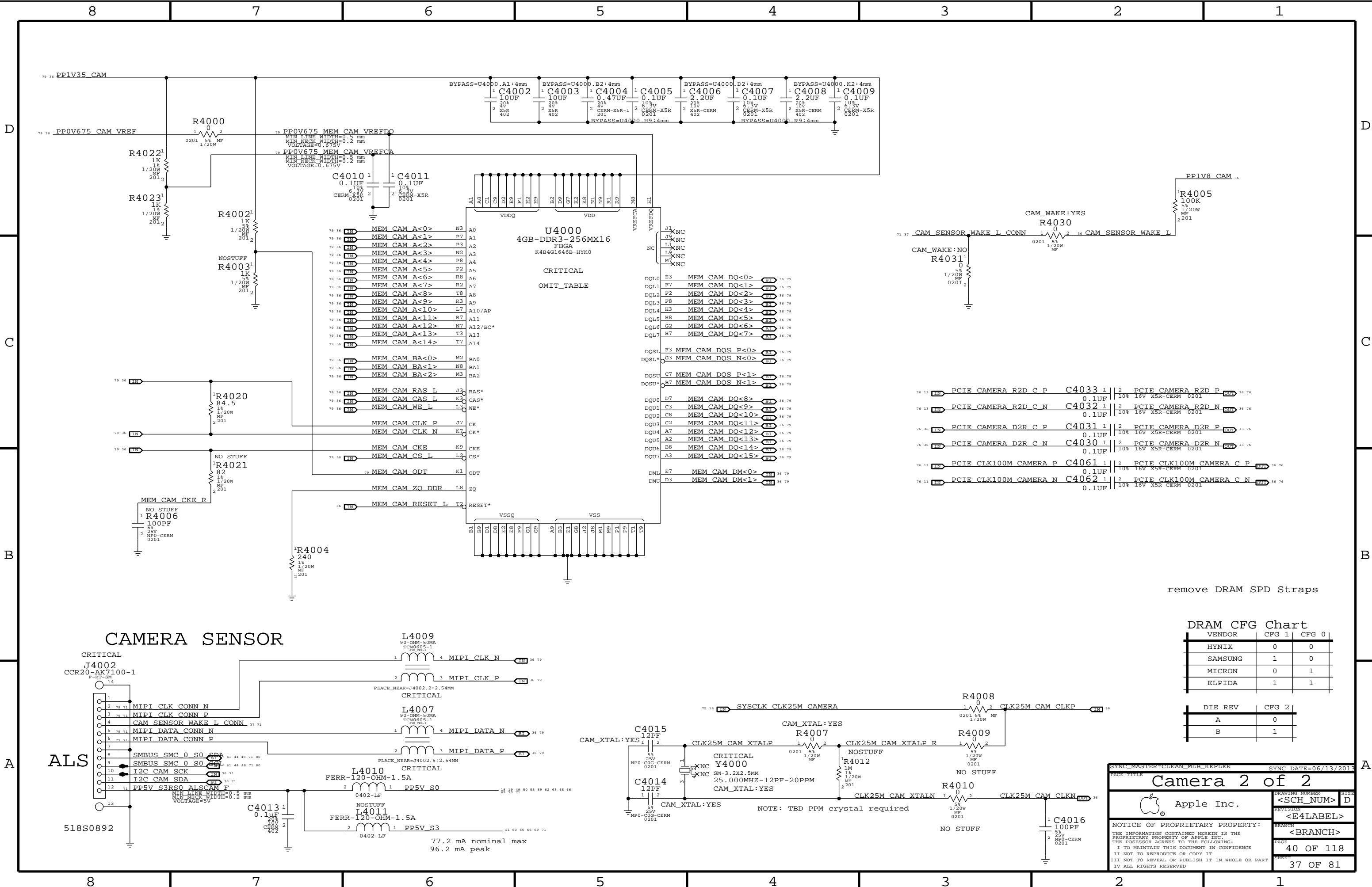
B

A



SYNC MASTER=CLEAN MLB KEPLER		SYNC DATE=06/08/2013		
PAGE TITLE				
SSD Connector				
	DRAWING NUMBER		SIZE	
	<SCH_NUM>		D	
	REVISION		<E4LABEL>	
	BRANCH		<BRANCH>	
NOTICE OF PROPRIETARY PROPERTY:				
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:				
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE				
II NOT TO REPRODUCE OR COPY IT				
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART				
IV ALL RIGHTS RESERVED				
PAGE		37 OF 118		
SHEET		35 OF 81		





PCIE CAMERA R2D C P	C4033	1	2	PCIE CAMERA R2D P	36	76
		0.1UF	10%	16V X5R-CERM 0201	36	76
PCIE CAMERA R2D C N	C4032	1	2	PCIE CAMERA R2D N	36	76
		0.1UF	10%	16V X5R-CERM 0201	36	76
PCIE CAMERA D2R C P	C4031	1	2	PCIE CAMERA D2R P	13	76
		0.1UF	10%	16V X5R-CERM 0201	13	76
PCIE CAMERA D2R C N	C4030	1	2	PCIE CAMERA D2R N	13	76
		0.1UF	10%	16V X5R-CERM 0201	13	76
PCIE CLK100M CAMERA P	C4061	1	2	PCIE CLK100M CAMERA C P	36	76
		0.1UF	10%	16V X5R-CERM 0201	36	76
PCIE CLK100M CAMERA N	C4062	1	2	PCIE CLK100M CAMERA C N	36	76
		0.1UF	10%	16V X5R-CERM 0201	36	76

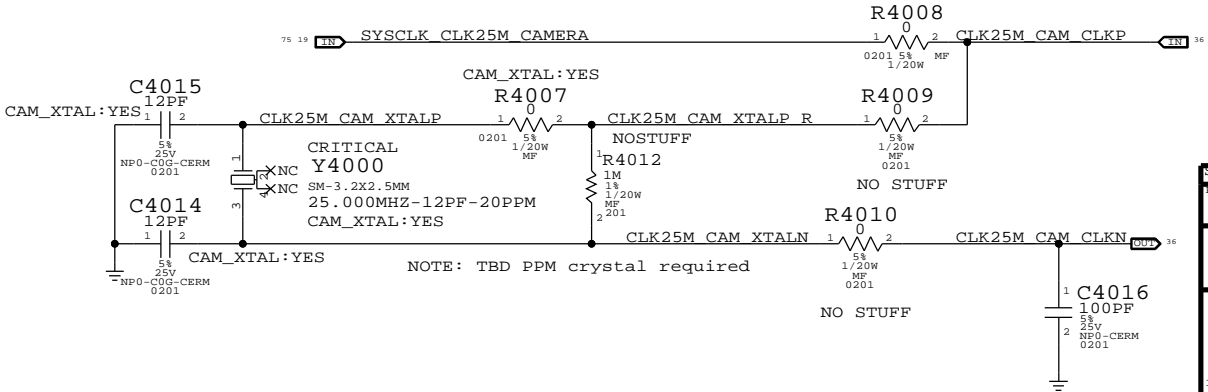
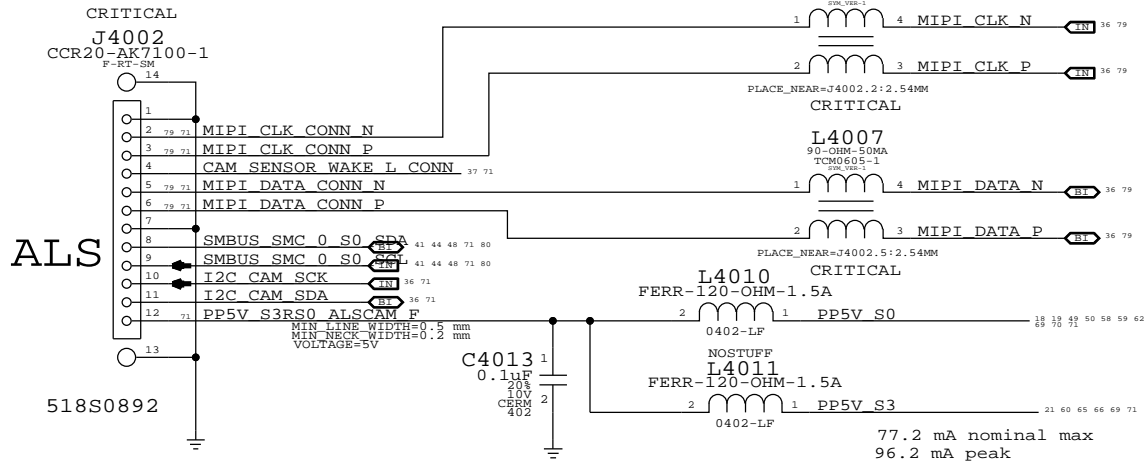
remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR



Camera 2 of 2

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

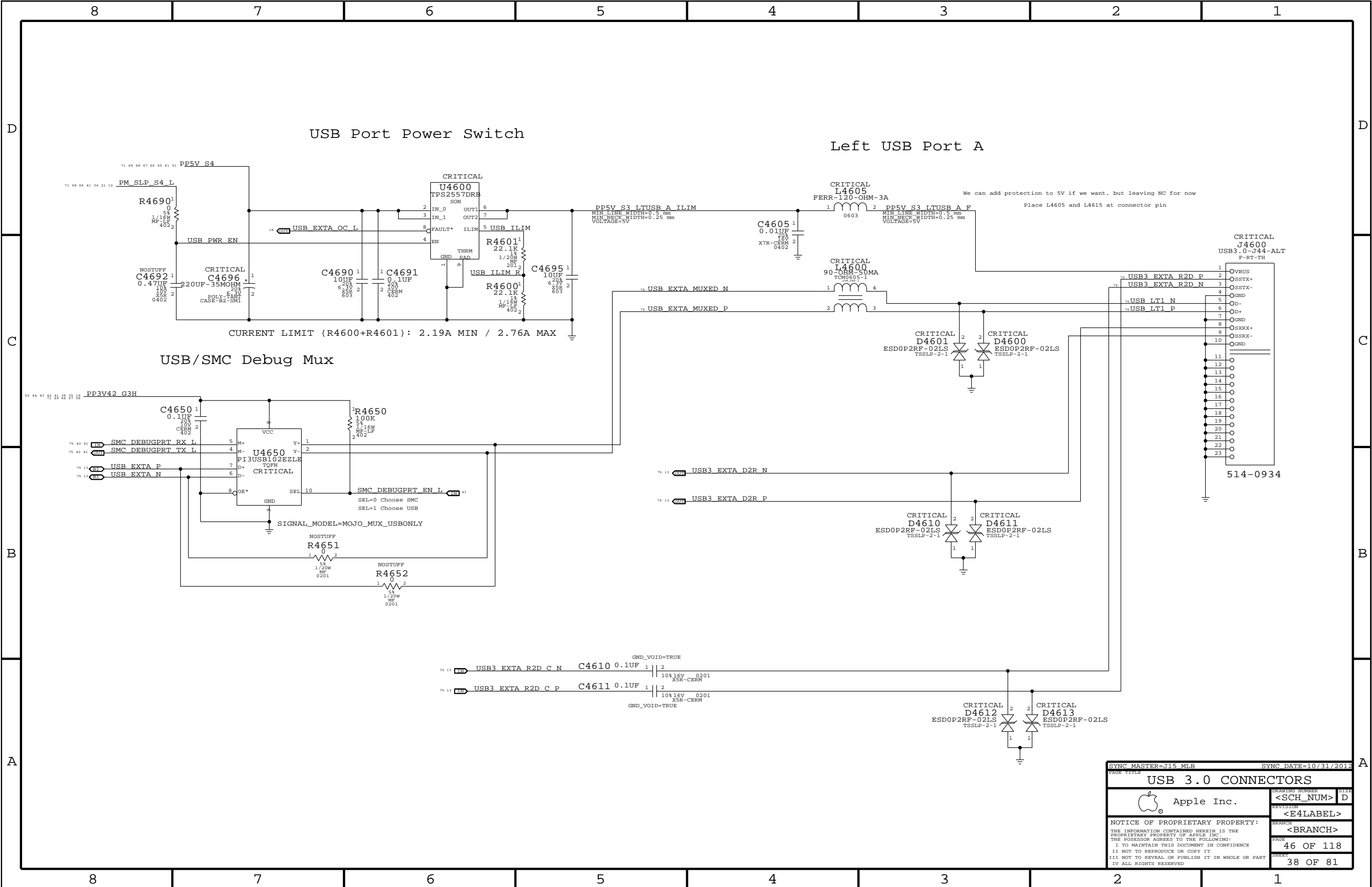
DRAWING NUMBER
<SCH_NUM> D

REVISION
<E4LABEL>

BRANCH
<BRANCH>

PAGE
40 OF 118

SHEET
37 OF 81



D

D

C

C

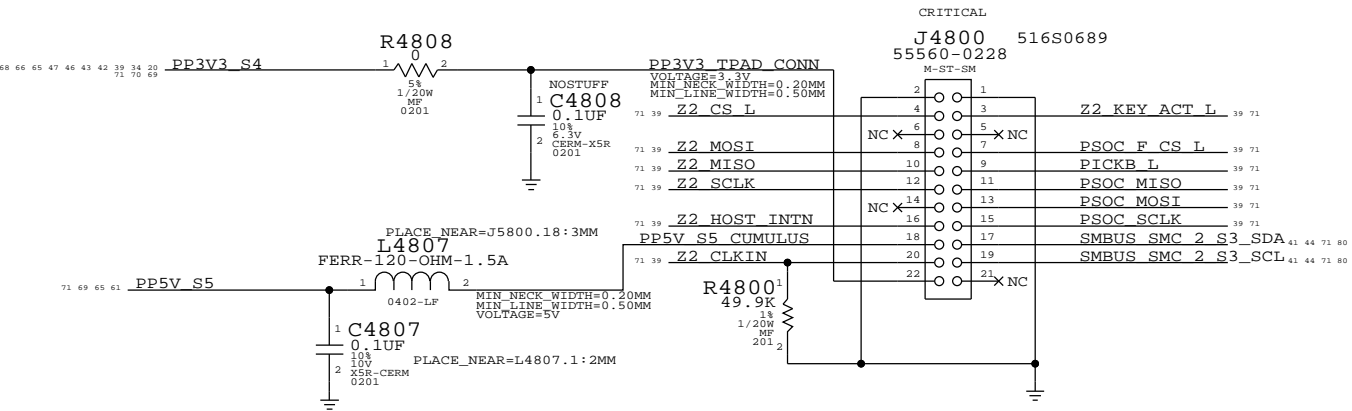
B

B

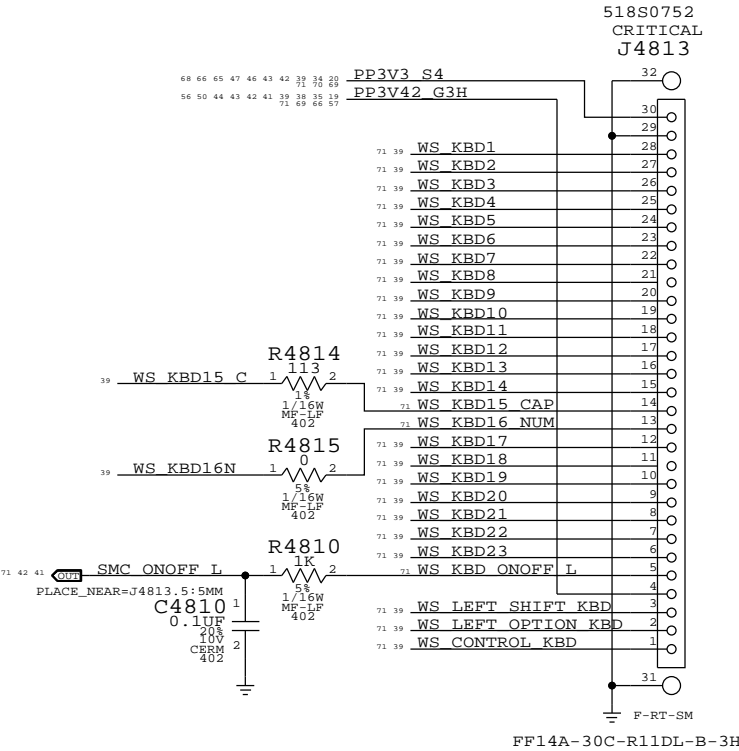
A

A

IPD Flex Connector

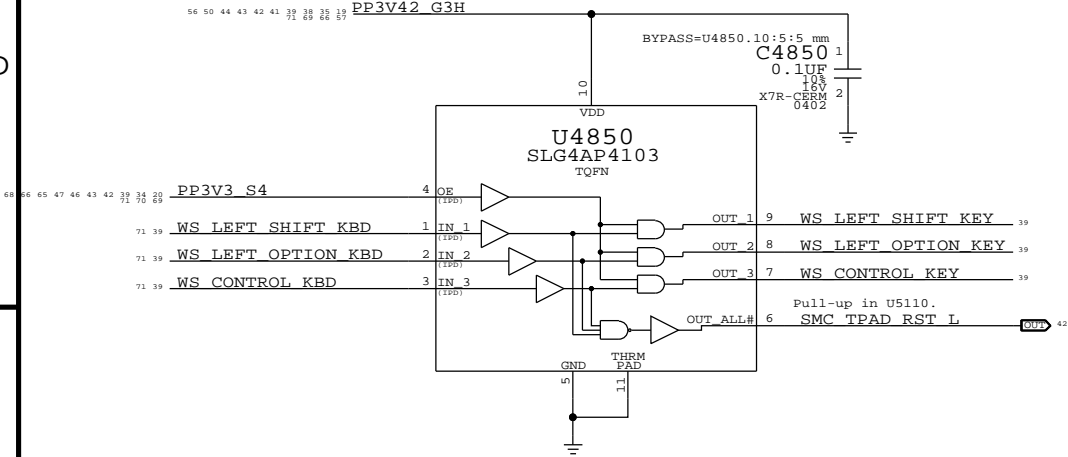


Keyboard Connector



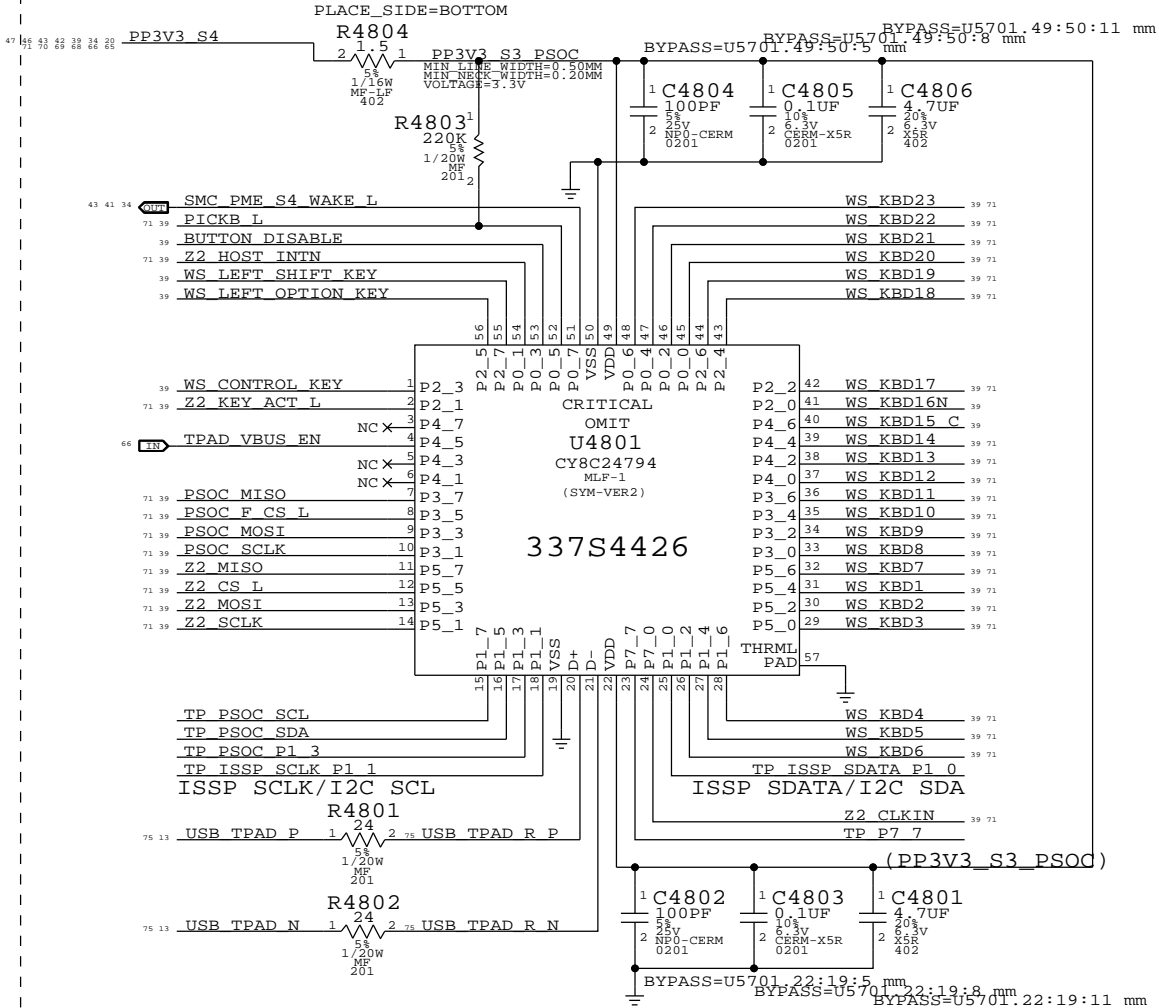
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

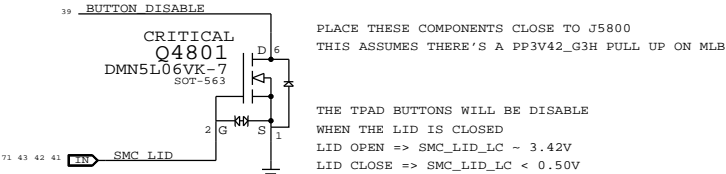


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



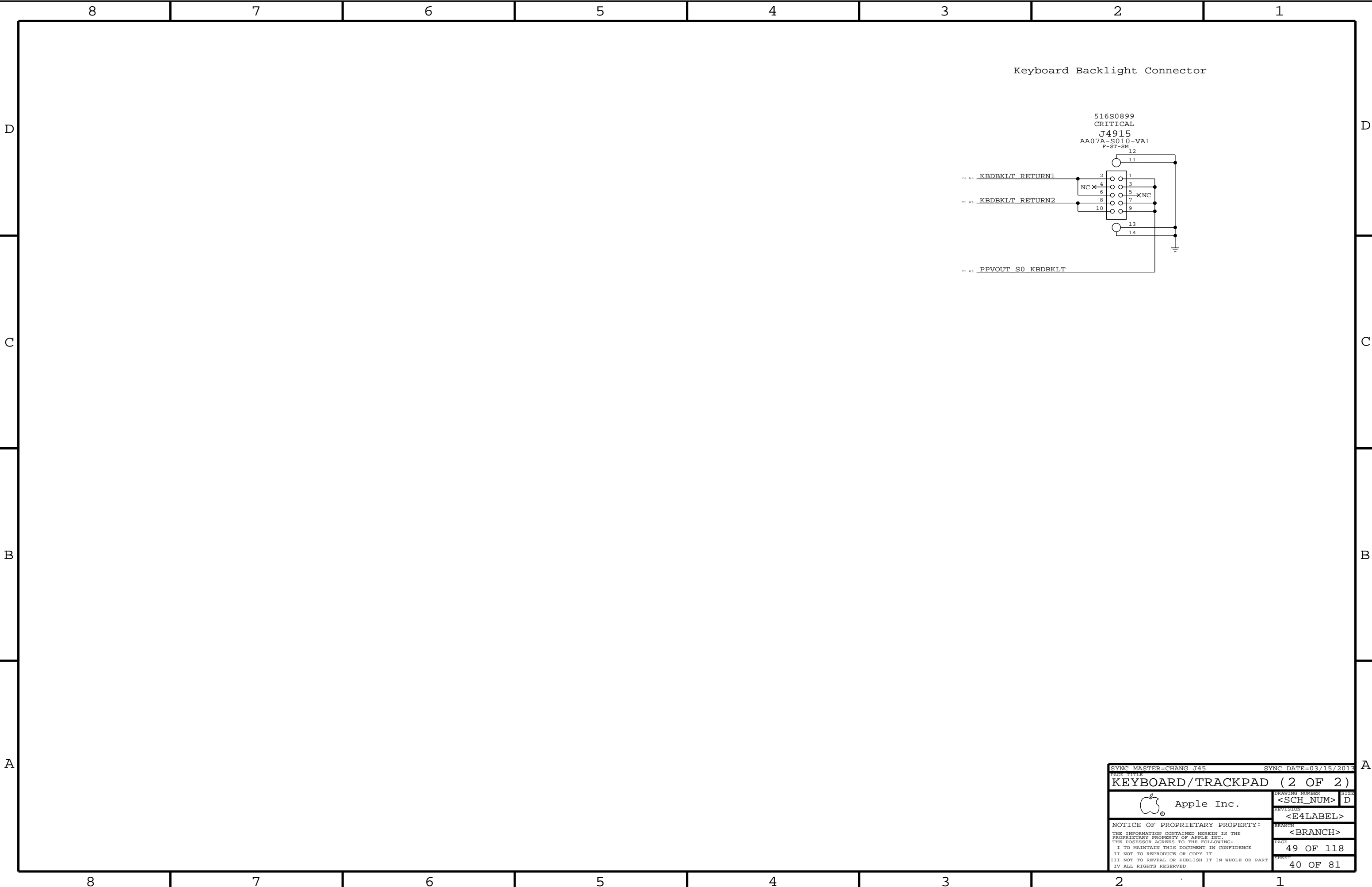
TPAD Buttons Disable

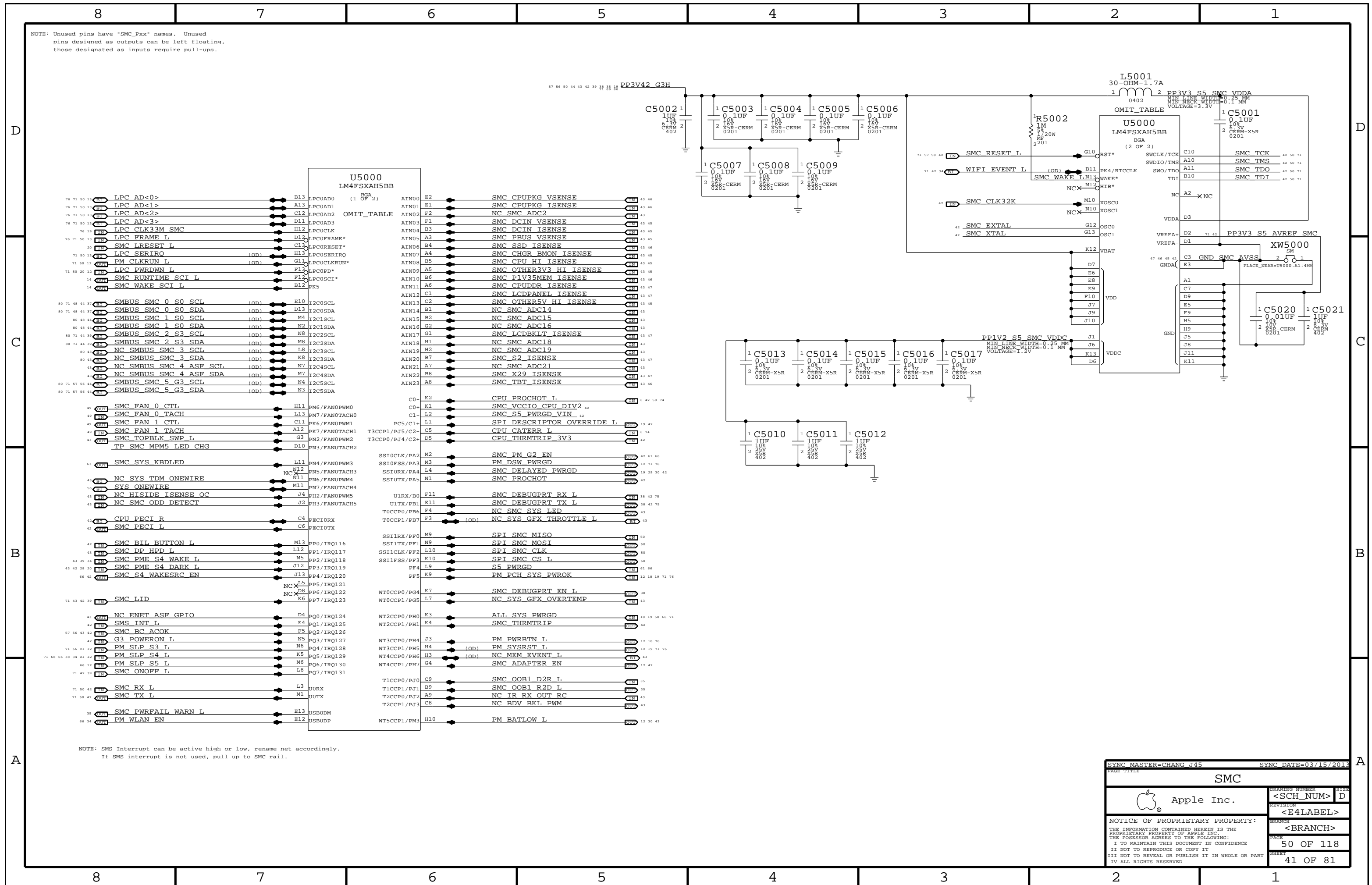


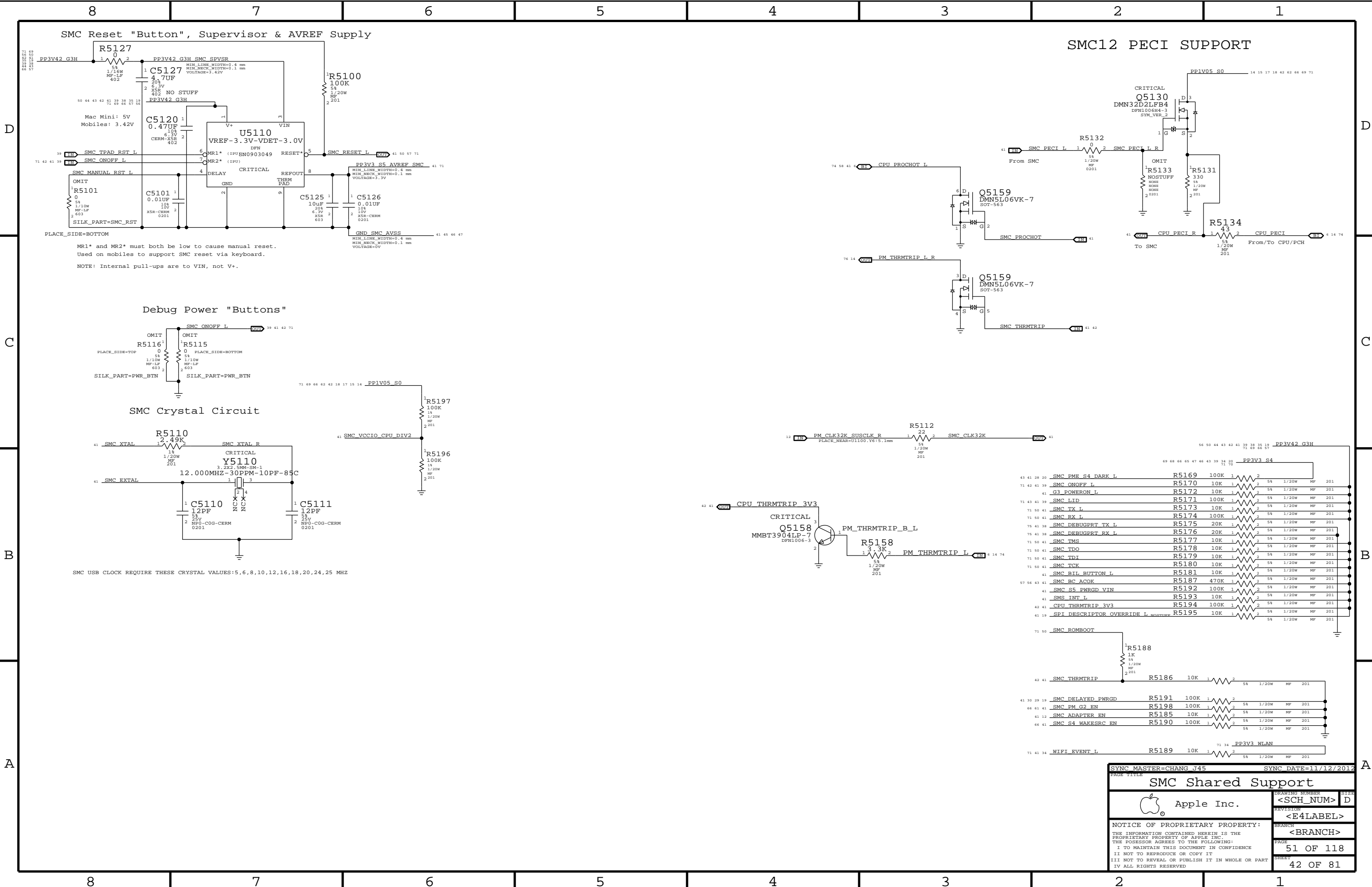
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN	NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W	
		80UA		0.204 V	16.32E-6 W	
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W	
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W	
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W	
		14MA (MAX)		0.021 V	294E-6 W	
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W	







SMC12 Peci Support

43 41 28 20	SMC PME S4 DARK L	R5169	100K	1	2				
71 42 41 39	SMC ONOFF L	R5170	10K	1	2	5%	1/20W	MF	201
41	G3 POWERON L	R5172	10K	1	2	5%	1/20W	MF	201
71 43 41 39	SMC LID	R5171	100K	1	2	5%	1/20W	MF	201
71 50 41	SMC TX L	R5173	10K	1	2	5%	1/20W	MF	201
71 50 41	SMC RX L	R5174	100K	1	2	5%	1/20W	MF	201
75 41 38	SMC DEBUGPRT TX L	R5175	20K	1	2	5%	1/20W	MF	201
75 41 38	SMC DEBUGPRT RX L	R5176	20K	1	2	5%	1/20W	MF	201
71 50 41	SMC TMS	R5177	10K	1	2	5%	1/20W	MF	201
71 50 41	SMC TDO	R5178	10K	1	2	5%	1/20W	MF	201
71 50 41	SMC TDI	R5179	10K	1	2	5%	1/20W	MF	201
71 50 41	SMC TCK	R5180	10K	1	2	5%	1/20W	MF	201
41	SMC BIL BUTTON L	R5181	10K	1	2	5%	1/20W	MF	201
57 56 43 41	SMC BC ACOK	R5187	470K	1	2	5%	1/20W	MF	201
41	SMC S5 PWRGD VIN	R5192	100K	1	2	5%	1/20W	MF	201
41	SMC INT L	R5193	10K	1	2	5%	1/20W	MF	201
42 41	CPU THRMTRIP 3V3	R5194	100K	1	2	5%	1/20W	MF	201
41 19	SPI DESCRIPTOR OVERRIDE L	R5195	10K	1	2	5%	1/20W	MF	201
71 50	SMC ROMBOOT	R5188	1K	1	2	5%	1/20W	MF	201
42 41	SMC THRMTRIP	R5186	10K	1	2	5%	1/20W	MF	201
41 30 29 19	SMC DELAYED PWRGD	R5191	100K	1	2	5%	1/20W	MF	201
66 61 41	SMC PM G2 EN	R5198	100K	1	2	5%	1/20W	MF	201
41 12	SMC ADAPTER EN	R5185	10K	1	2	5%	1/20W	MF	201
66 41	SMC S4 WAKESRC EN	R5190	100K	1	2	5%	1/20W	MF	201
71 41 34	WIFI EVENT L	R5189	10K	1	2	5%	1/20W	MF	201

SYNC MASTER=CHANG J45

SYNC DATE=11/12/2012

SMC Shared Support

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

BRANCH

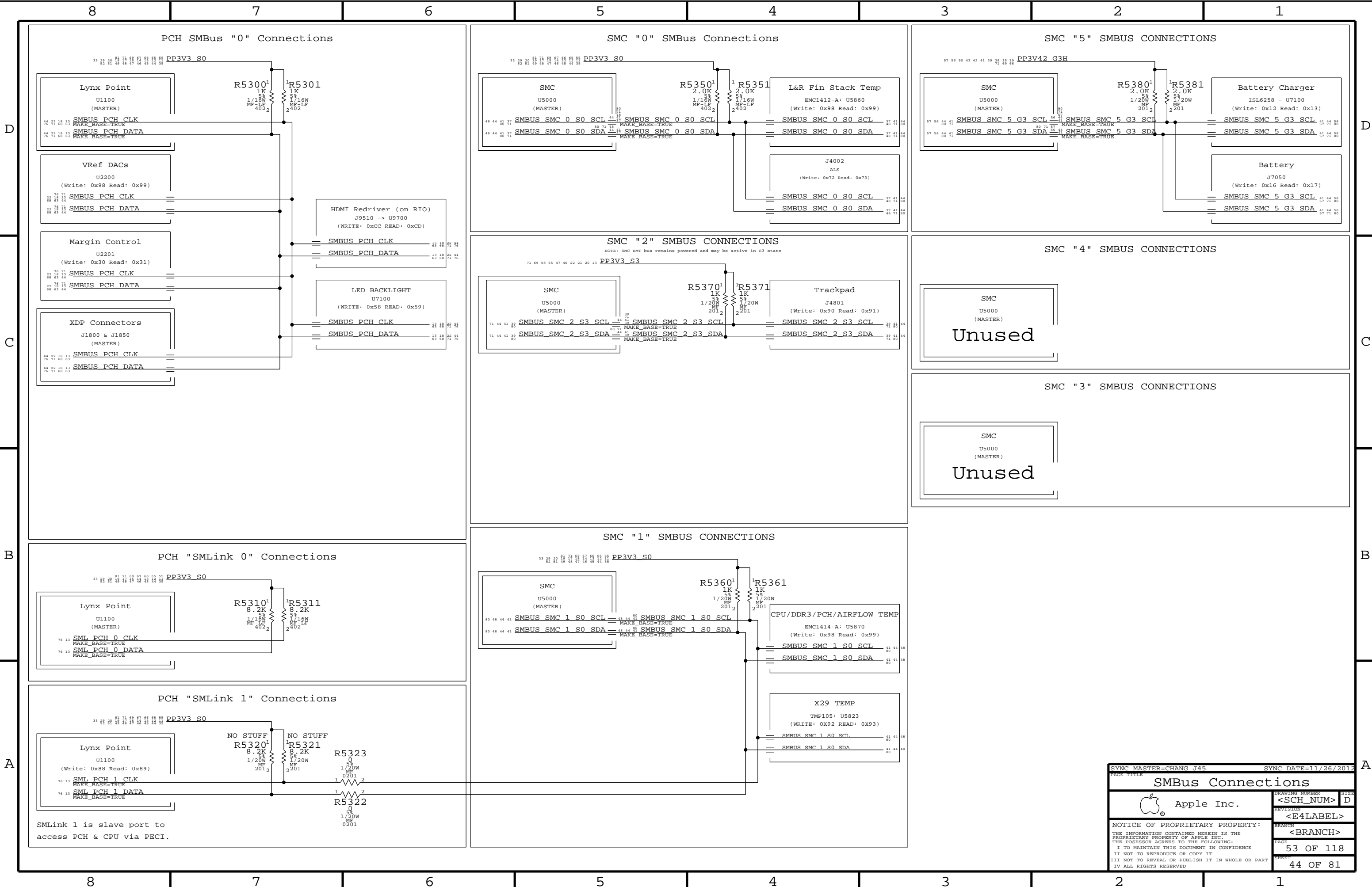
<BRANCH>

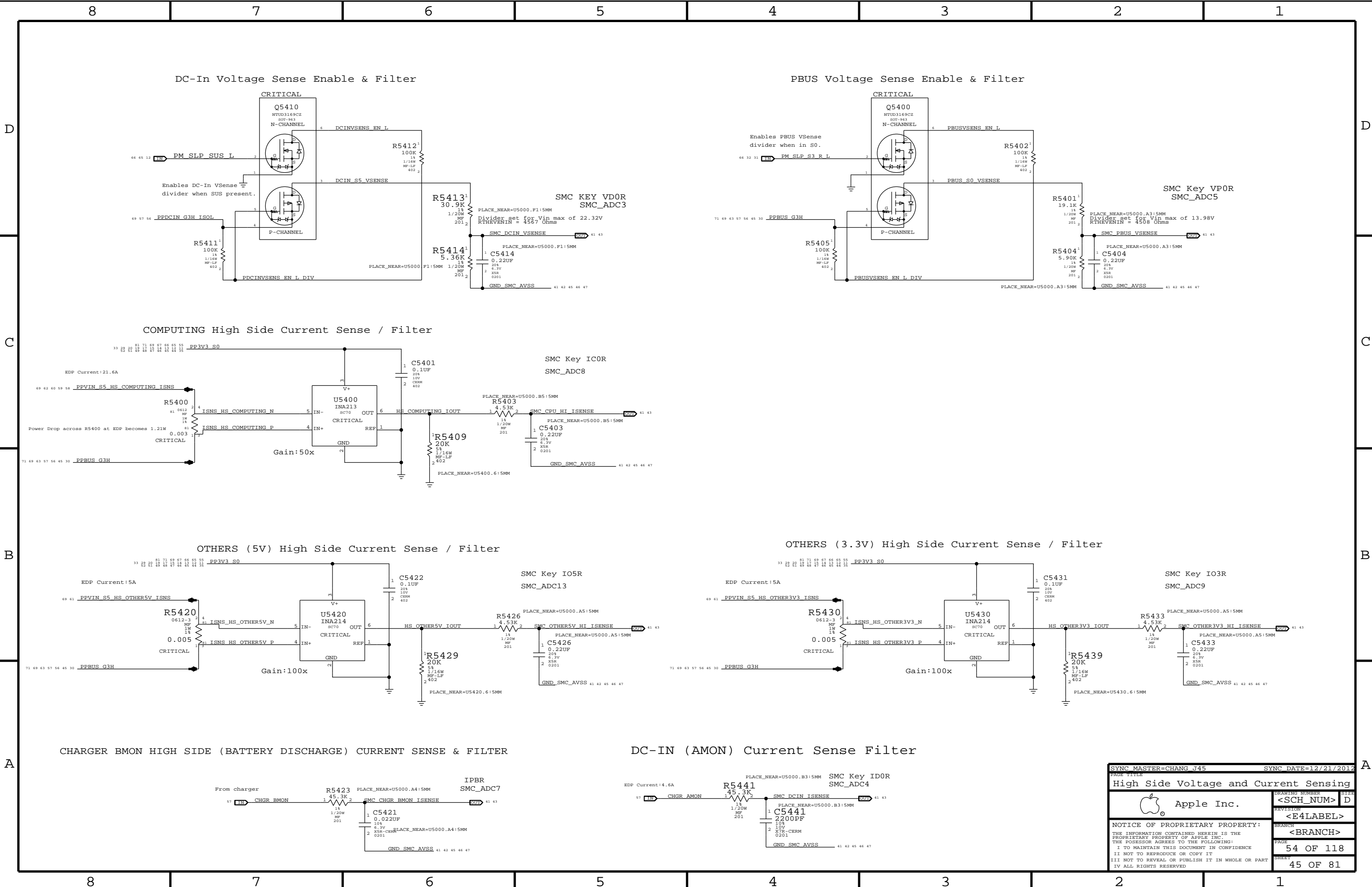
PAGE


51 OF 118

SHEET

42 OF 81





SYNC MASTER=CHANG J45		SYNC DATE=12/21/2012	
PAGE TITLE			
High Side Voltage and Current Sensing			
 Apple Inc.	DRAWING NUMBER	SIZE	
	<SCH_NUM>	D	
	REVISION	<E4LABEL>	
	BRANCH	<BRANCH>	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
PAGE		54 OF 118	
SHEET		45 OF 81	

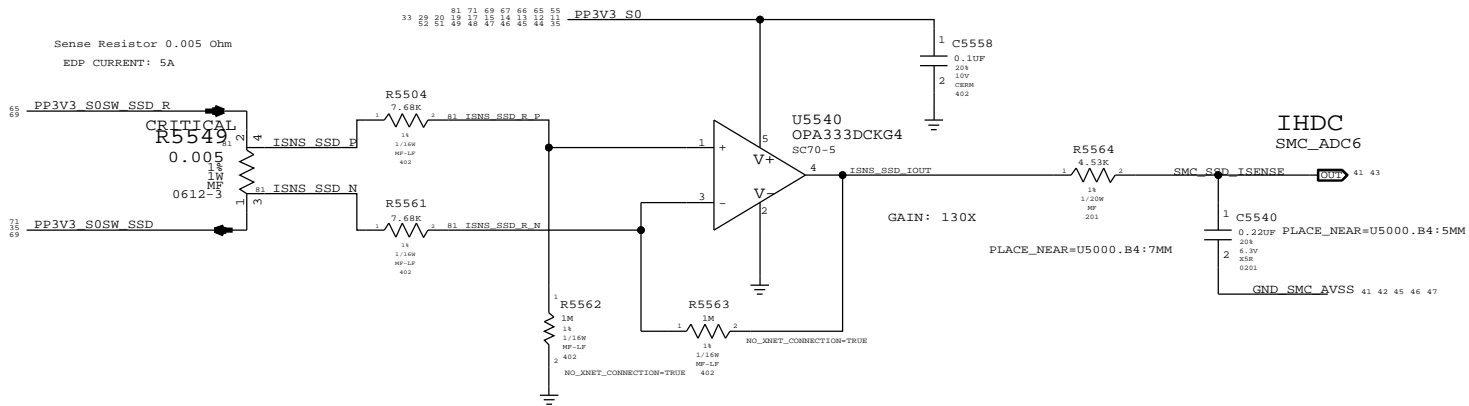
D

C

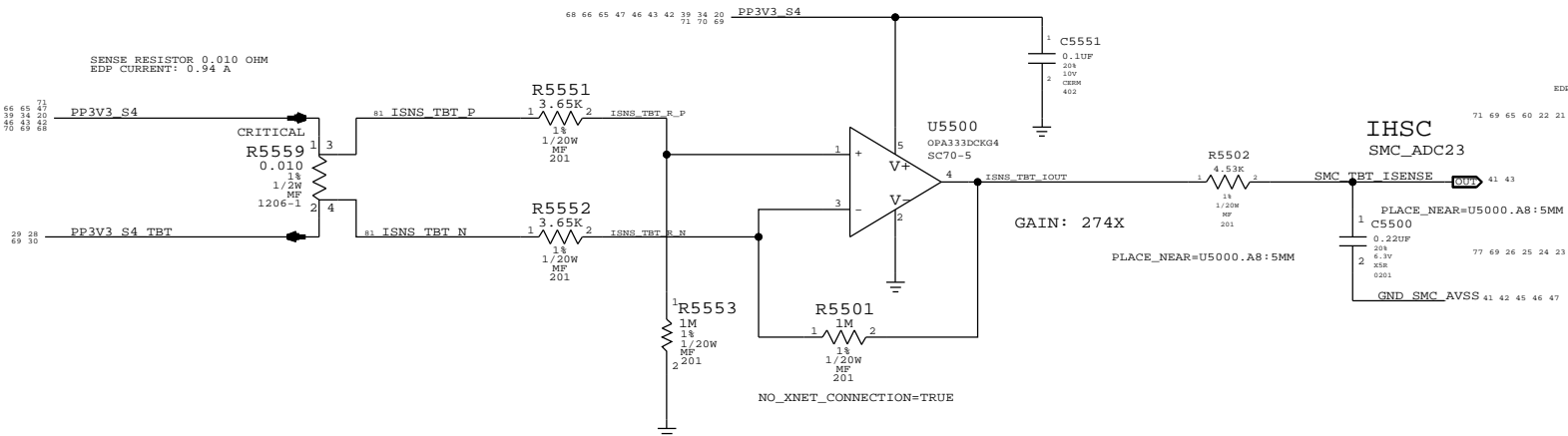
B

A

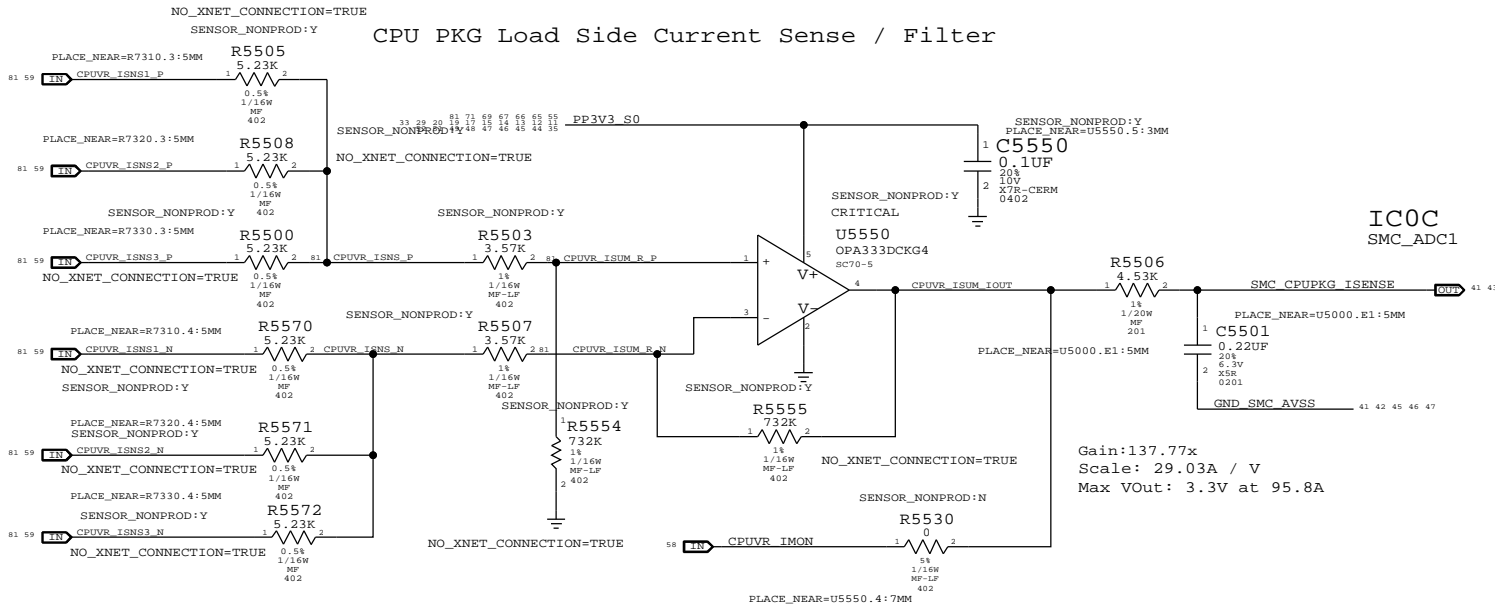
SSD CURRENT SENSE



TBT Router CURRENT SENSE

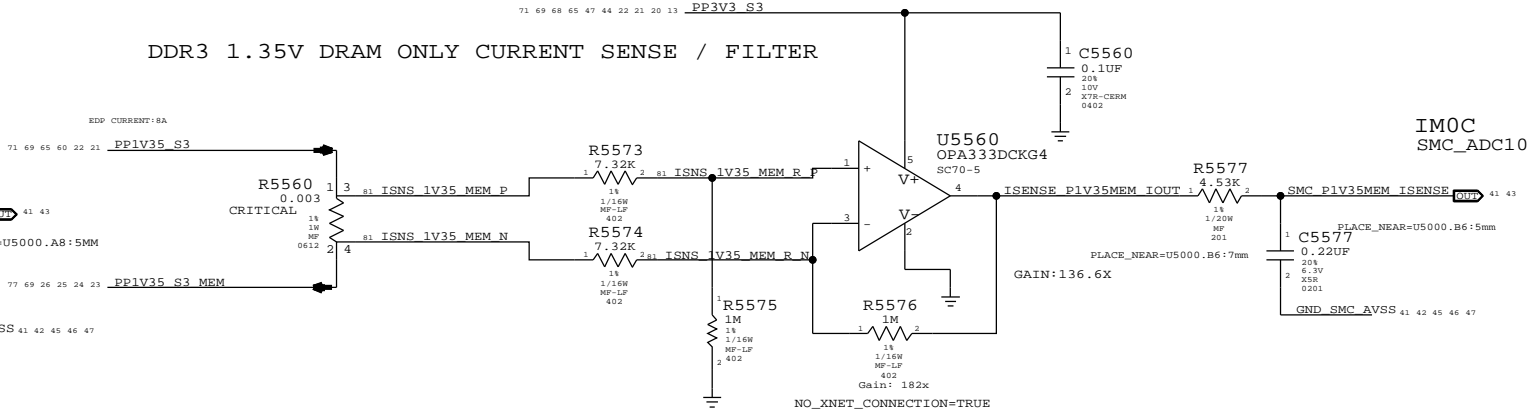


CPU PKG Load Side Current Sense / Filter

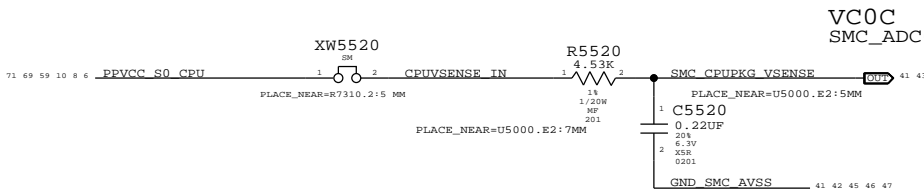



Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

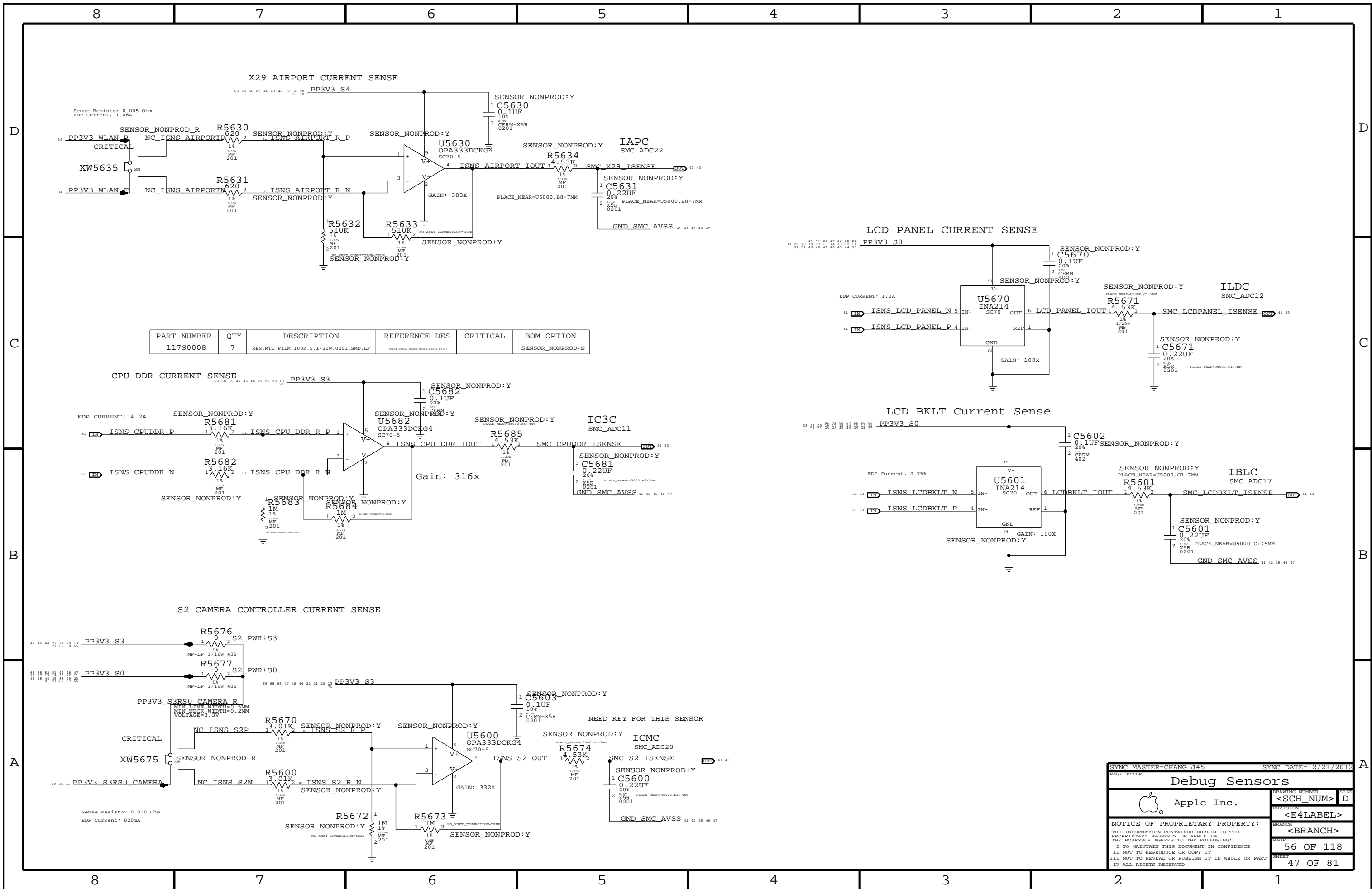
DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER

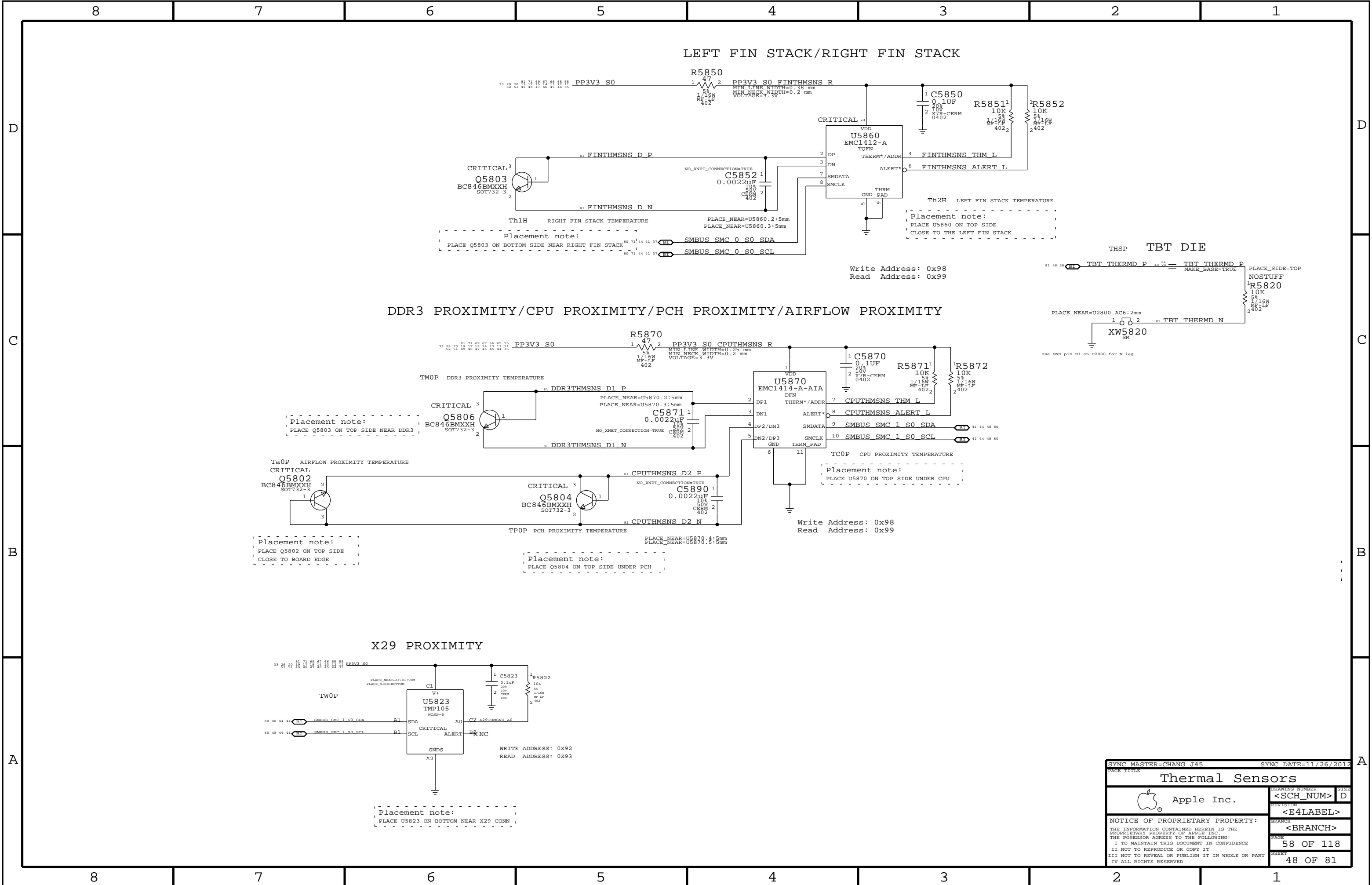



CPU Vcore Voltage Sense / Filter

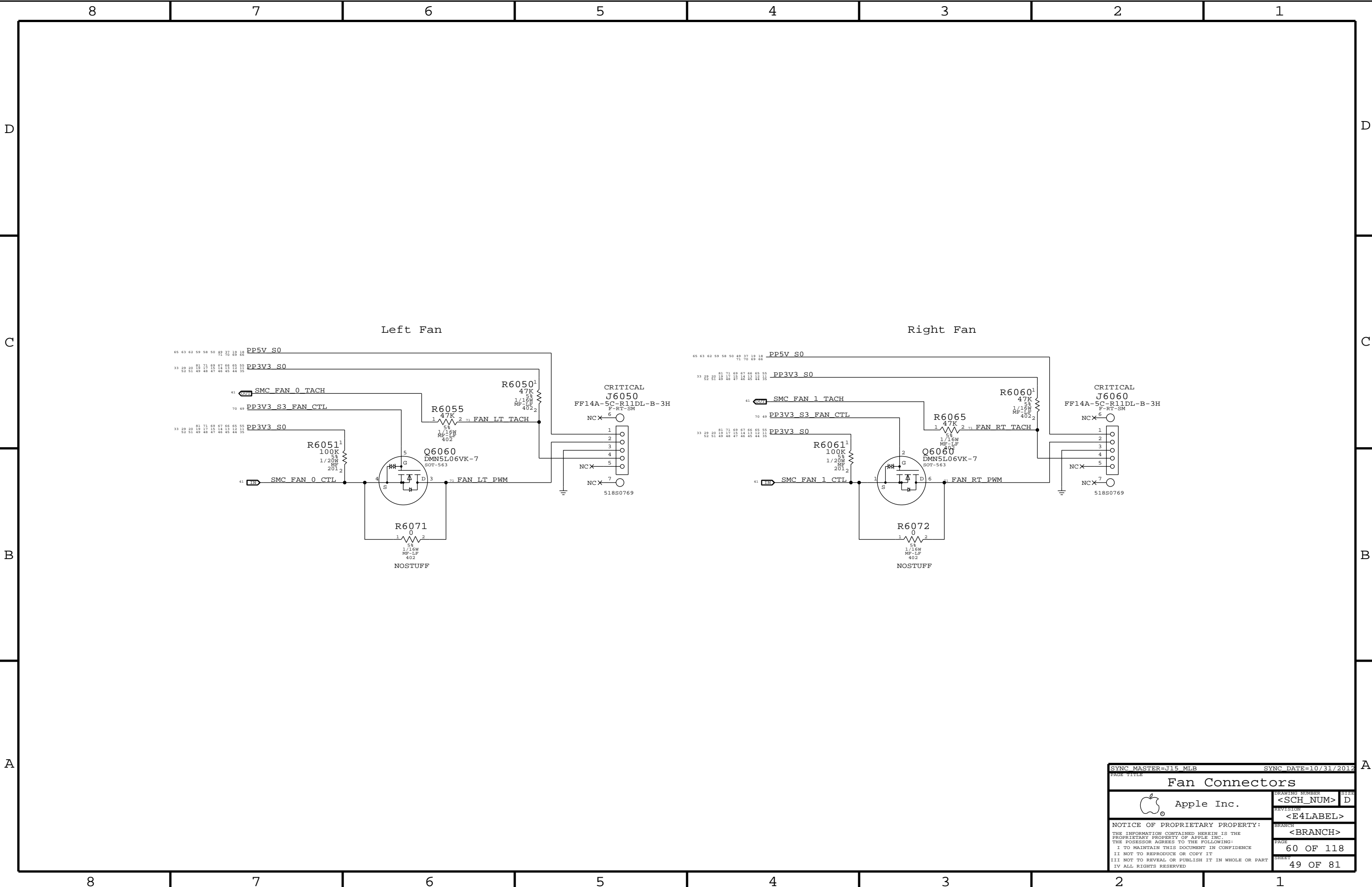


SYNC MASTER=CHANG J45		SYNC DATE=03/15/2013	
PAGE TITLE			
Load Side Voltage and Current Sensing			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		<BRANCH>	
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		PAGE	55 OF 118
II NOT TO REPRODUCE OR COPY IT		SHEET	46 OF 81
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			





SYNC MASTER=CHANG J45		SYNC DATE=11/26/2012	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	58 OF 118
		SHEET	48 OF 81



D

C

B

A

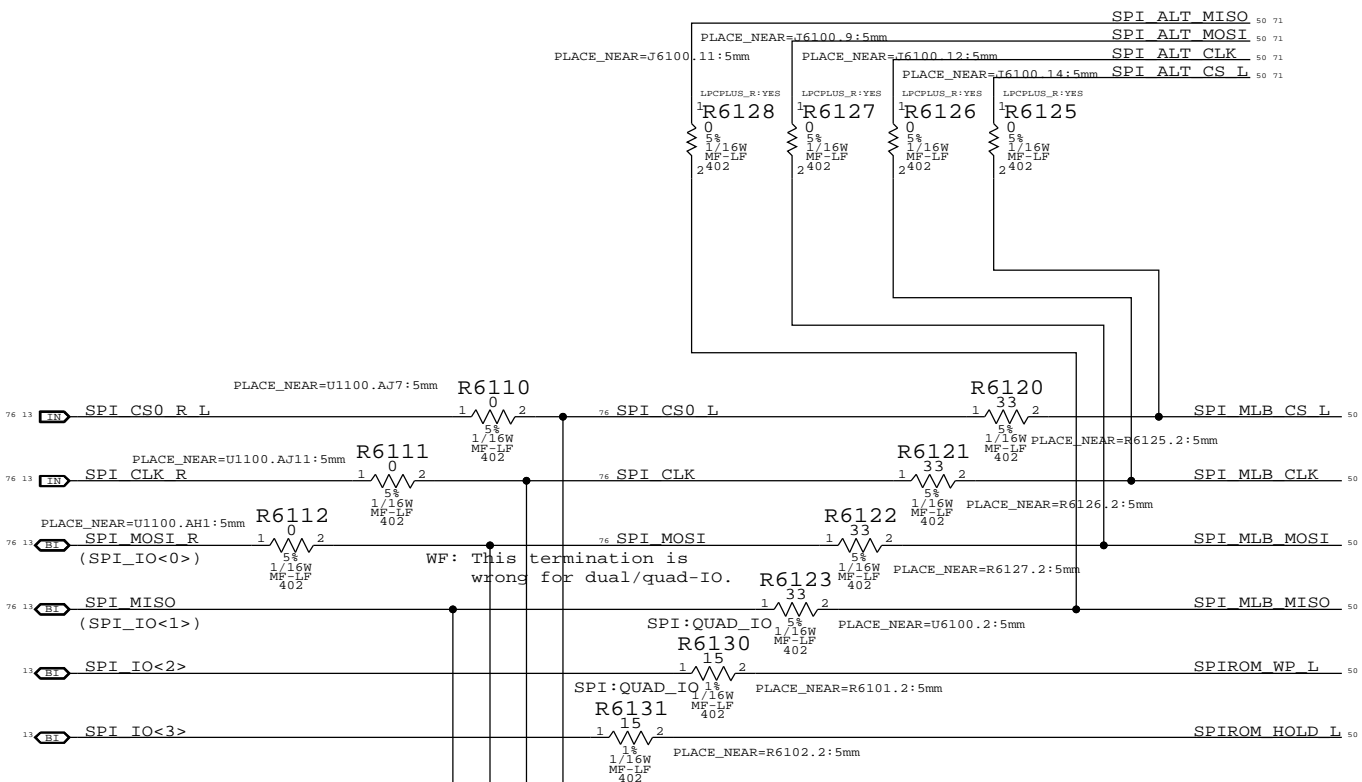
D

C

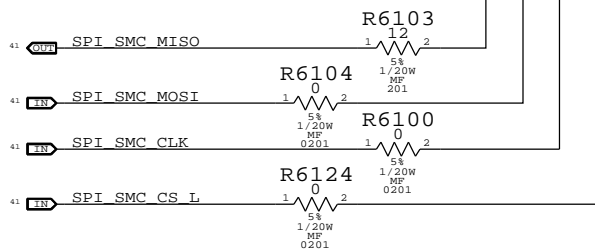
B

A

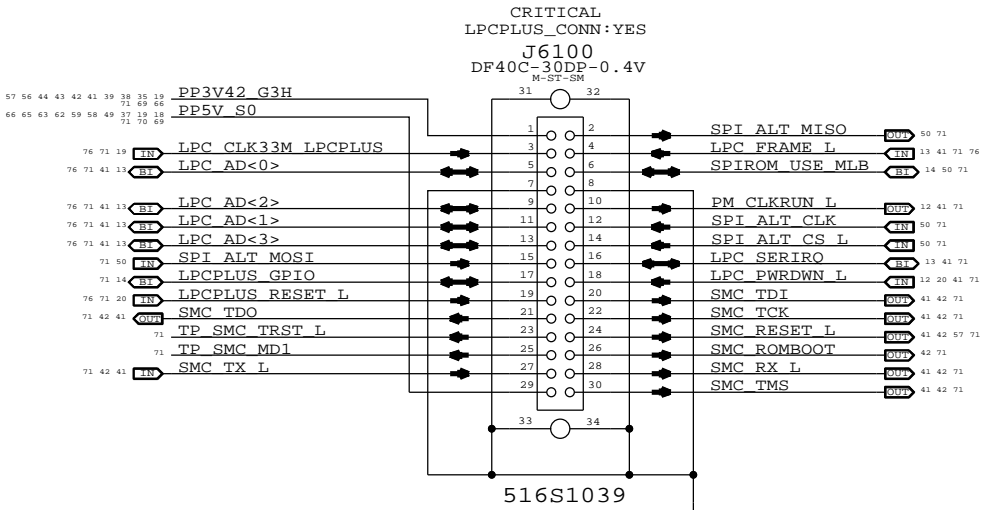
SPI Bus Series Termination



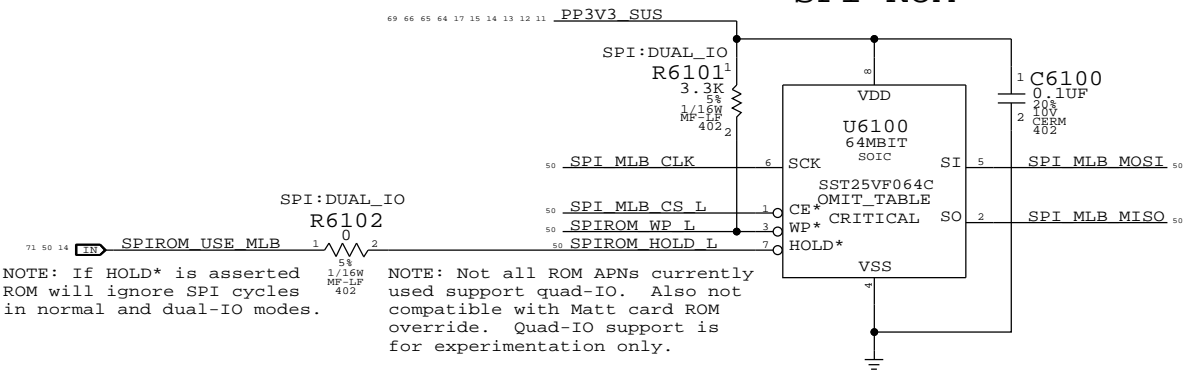
SMC12 SPI SUPPORT




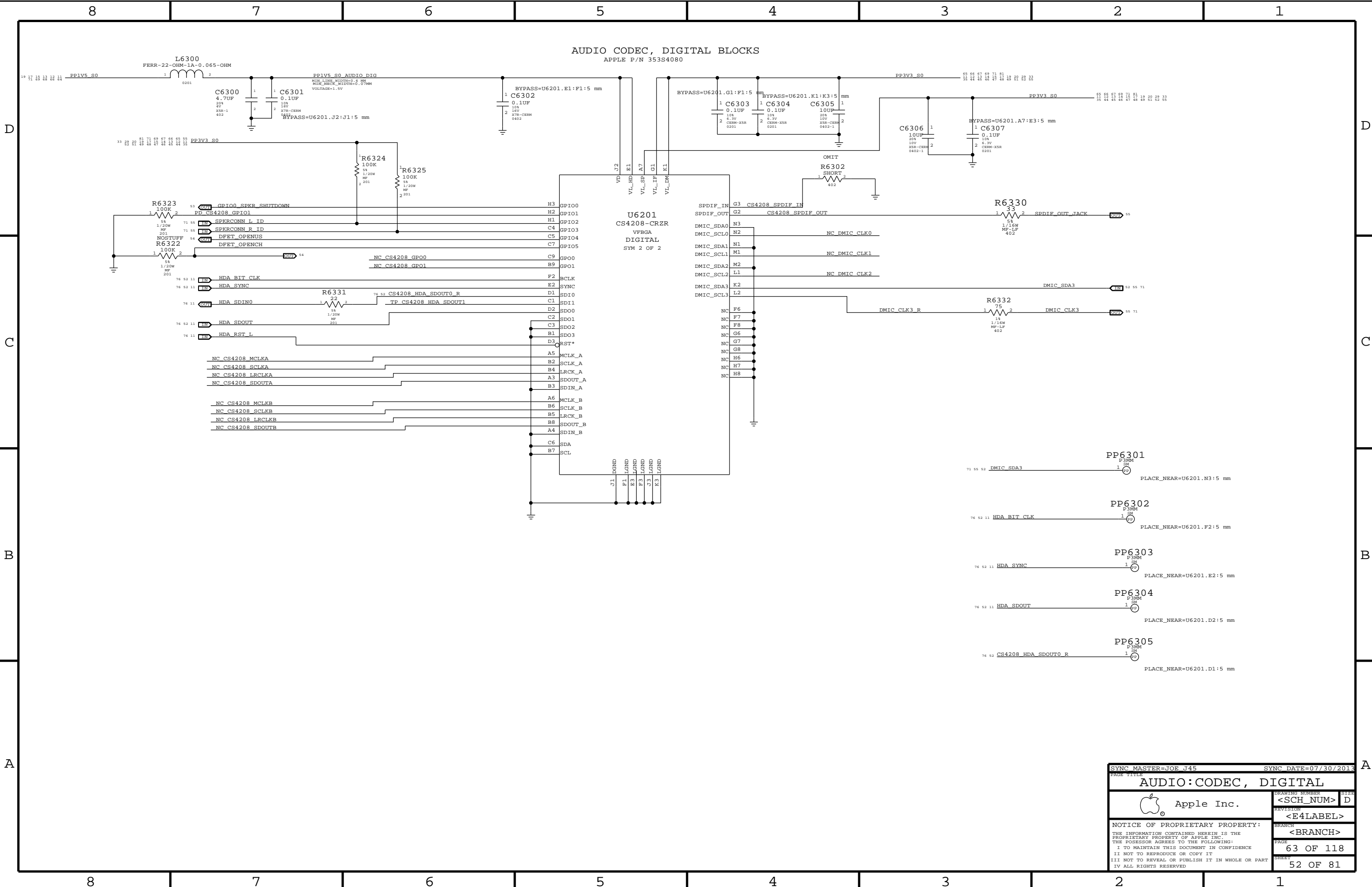
LPC+SPI Connector



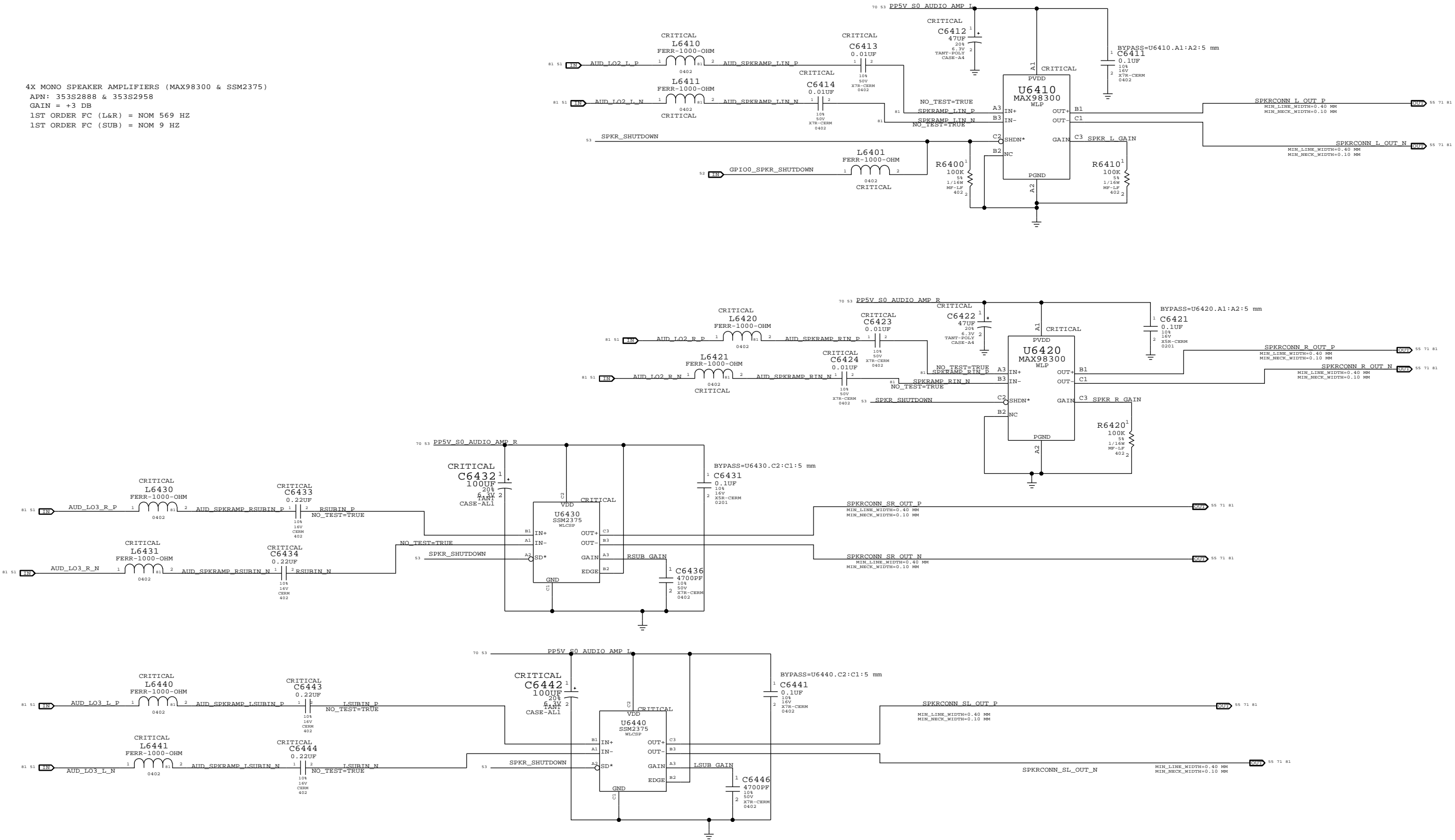
SPI ROM




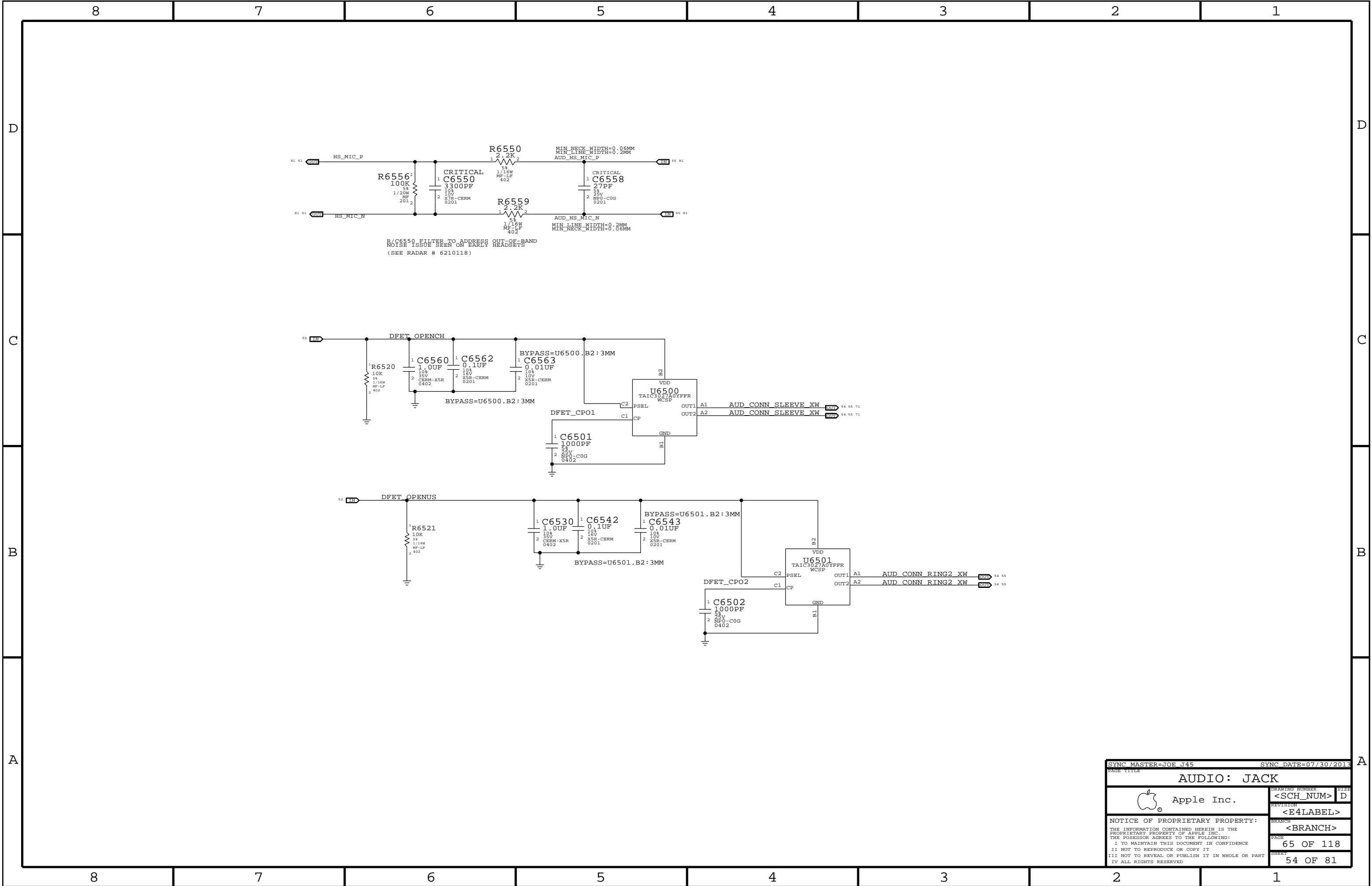
SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE			
SPI ROM / LPC+SPI Conn.			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	61 OF 118
		SHEET	50 OF 81

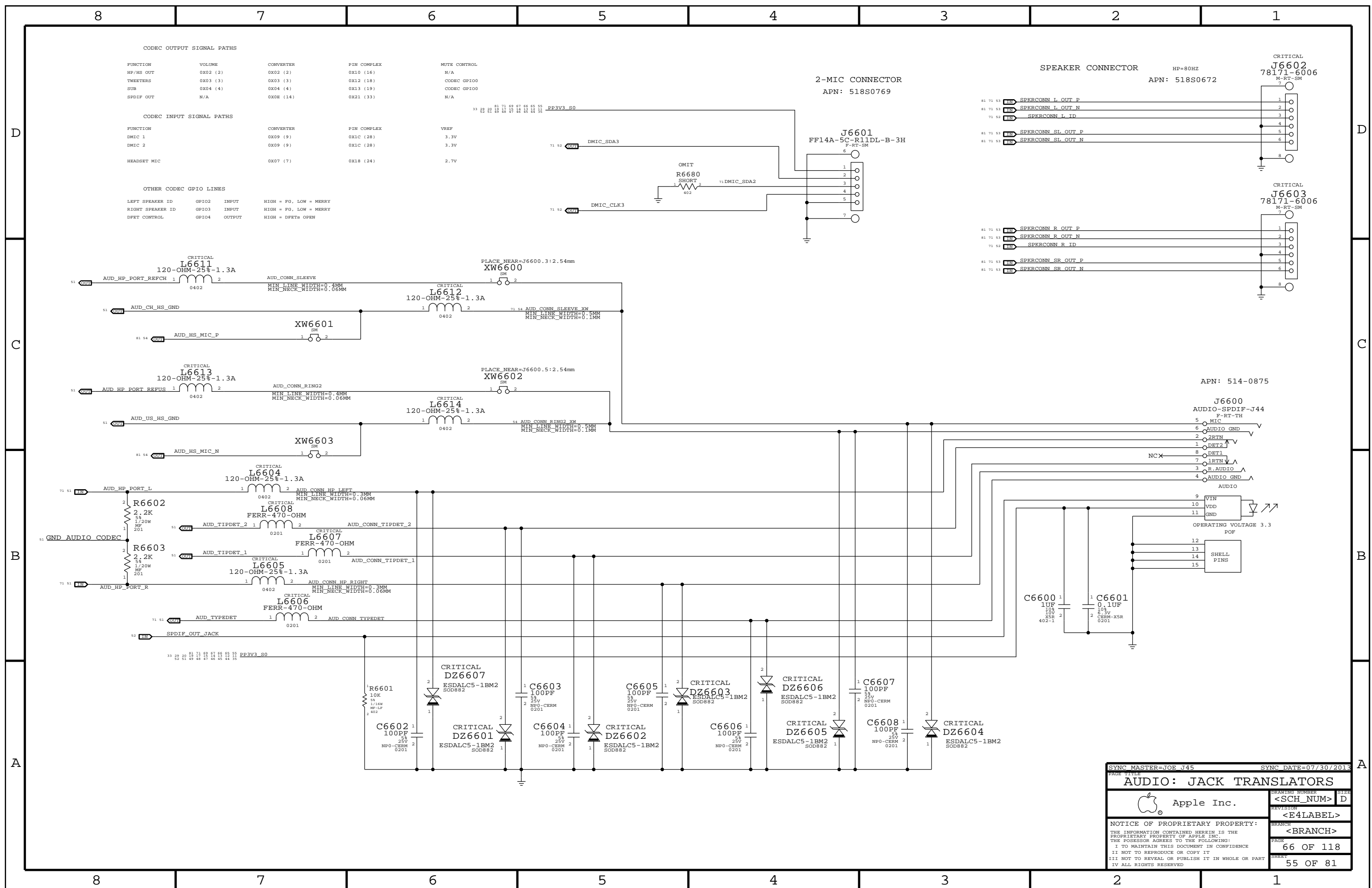


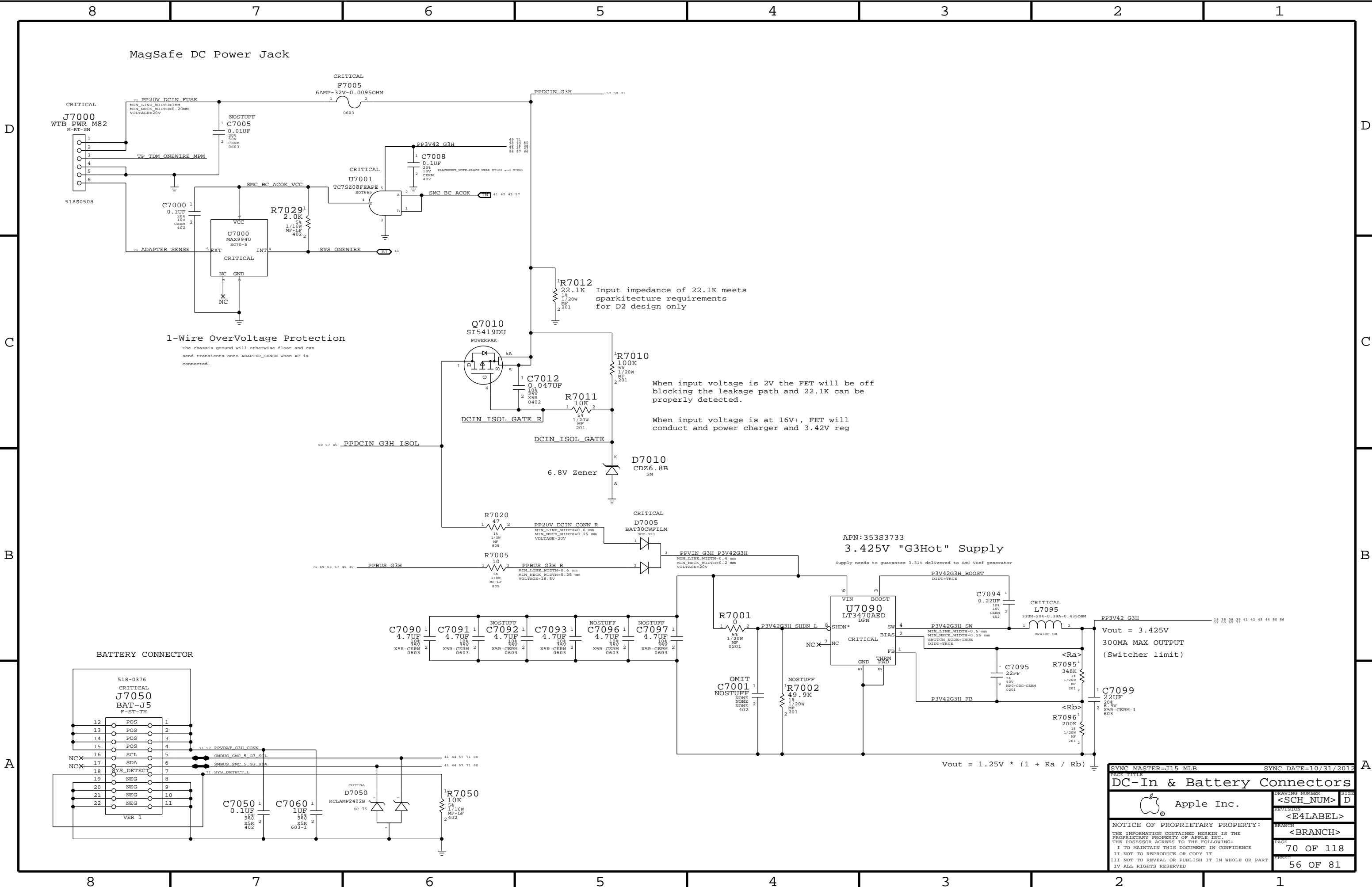
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	64 OF 118
		SHEET	53 OF 81







MagSafe DC Power Jack

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.


3.425V "G3Hot" Supply

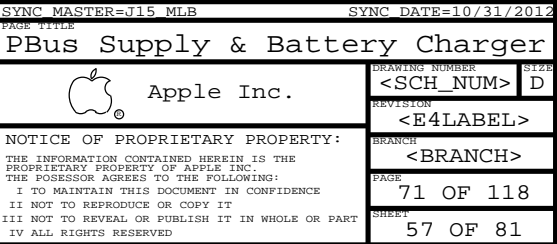
Supply needs to guarantee 3.31V delivered to SMC VRef generator

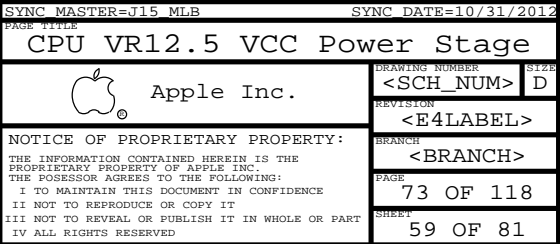
Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

BATTERY CONNECTOR

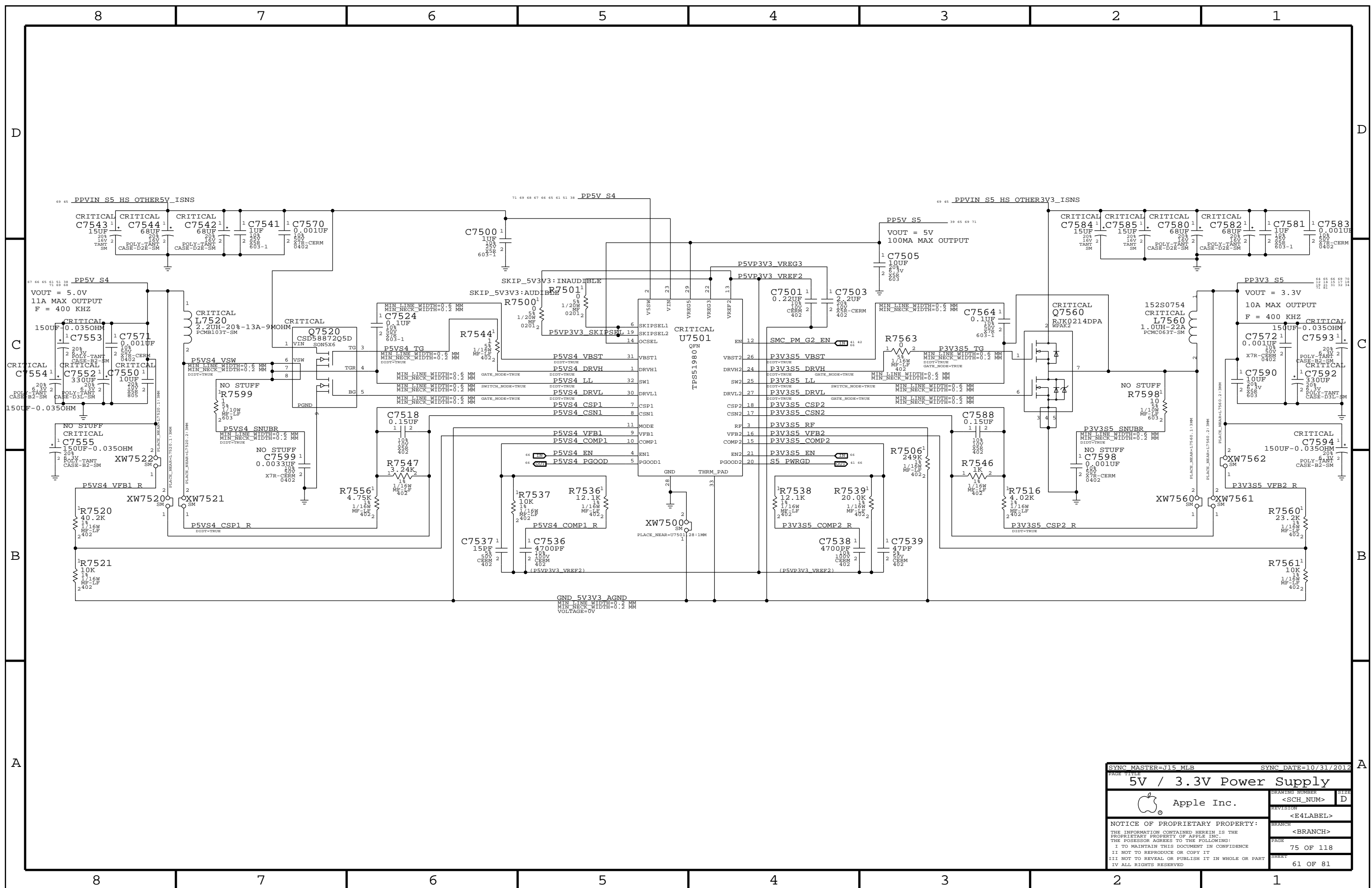
PAGE TITLE		DRAWING NUMBER		SIZE	
DC-In & Battery Connectors		<SCH_NUM>		D	
 Apple Inc.		REVISION		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH		<BRANCH>	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE		70 OF 118	
		SHEET		56 OF 81	



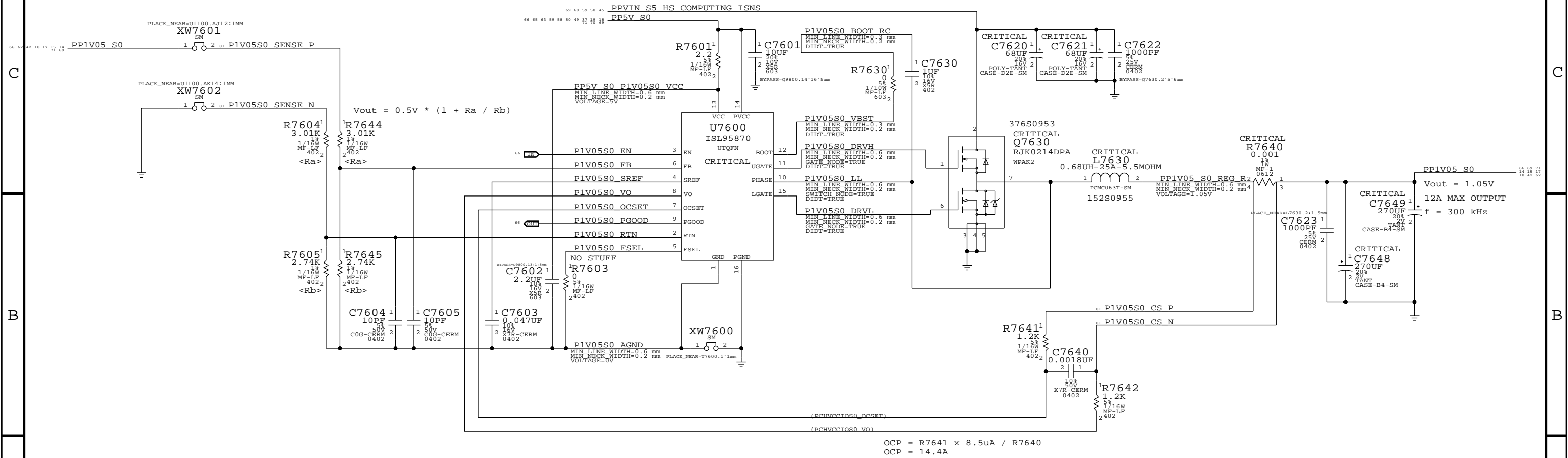


D


A



1V05 S0 REGULATOR



OCF = R7641 x 8.5uA / R7640
OCF = 14.4A

SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012		
PAGE TITLE				
1V05V POWER SUPPLY				
 Apple Inc.	DRAWING NUMBER		SIZE	
	<SCH_NUM>		D	
	REVISION		<E4LABEL>	
	BRANCH		<BRANCH>	
NOTICE OF PROPRIETARY PROPERTY:				
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:				
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE				
II NOT TO REPRODUCE OR COPY IT				
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART				
IV ALL RIGHTS RESERVED				
PAGE		76 OF 118		
SHEET		62 OF 81		

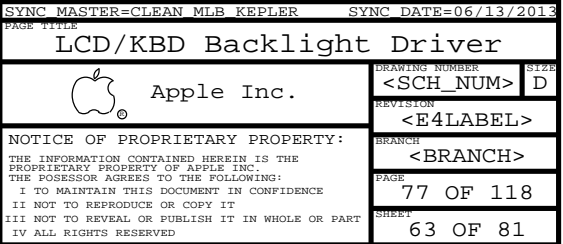
Power aliases required by this page:

- =PPVFN_S0_LCDCKLTL	(9-12.6V LCD Backlight Input)
- =PPVFN_S0_BKLCTCTRL	(5V Backlight Driver Input)
- =PPVFN_S0_KBDLED	(5V Keyboard Backlight Input)

BOM options provided by this page:

BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds

BKLT:PROD - Stuffs 0 ohm series R for production

[illegible]

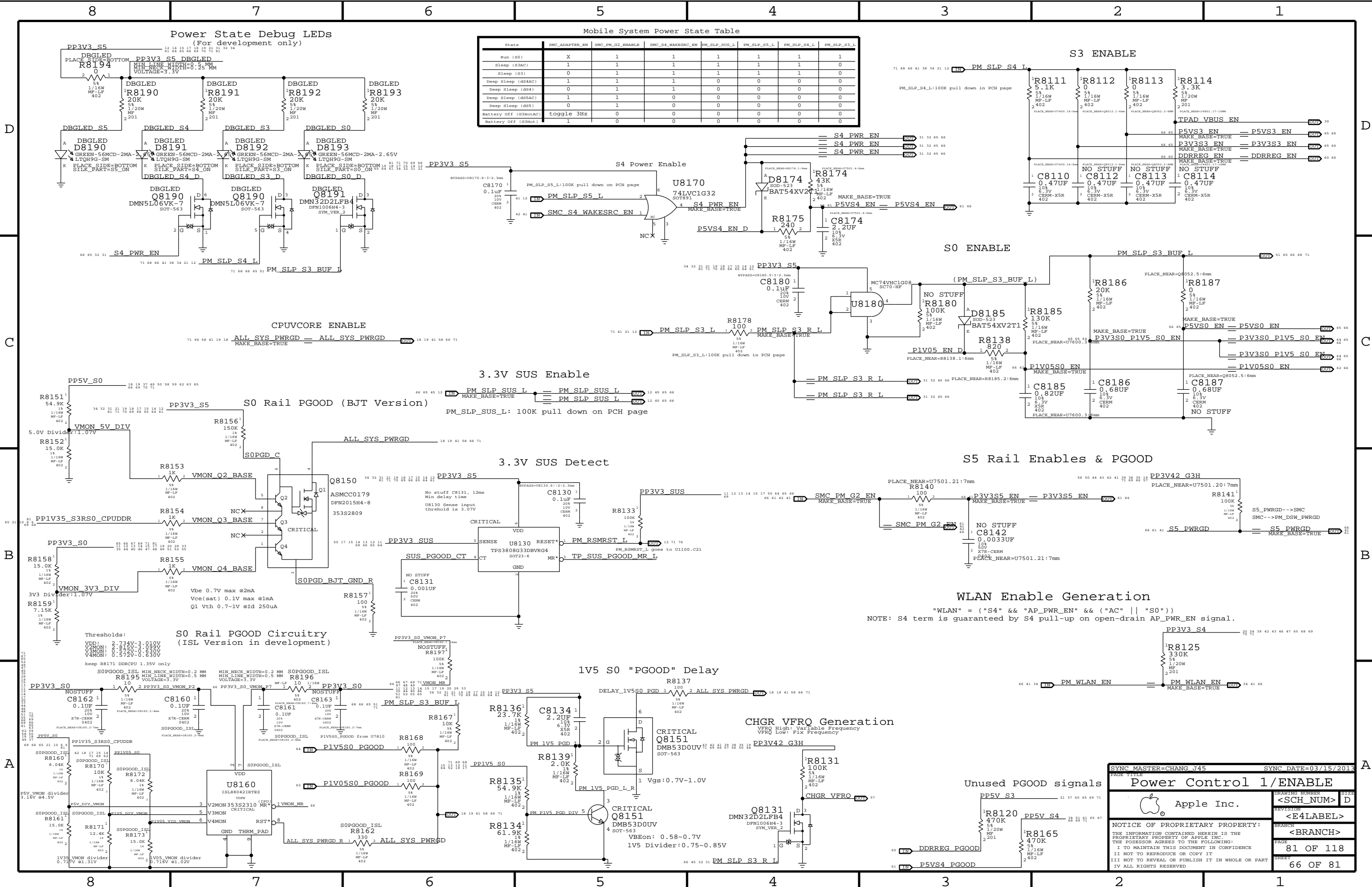
D



D

C

A



Mobile System Power State Table						
State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L
Run (S0)	X	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0
Deep Sleep (dS4C)	1	1	0	0	0	0
Deep Sleep (dS5)	1	1	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0

SYNC MASTER=CHANG J45

SYNC DATE=03/15/2013

Power Control 1/ENABLE

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

BRANCH

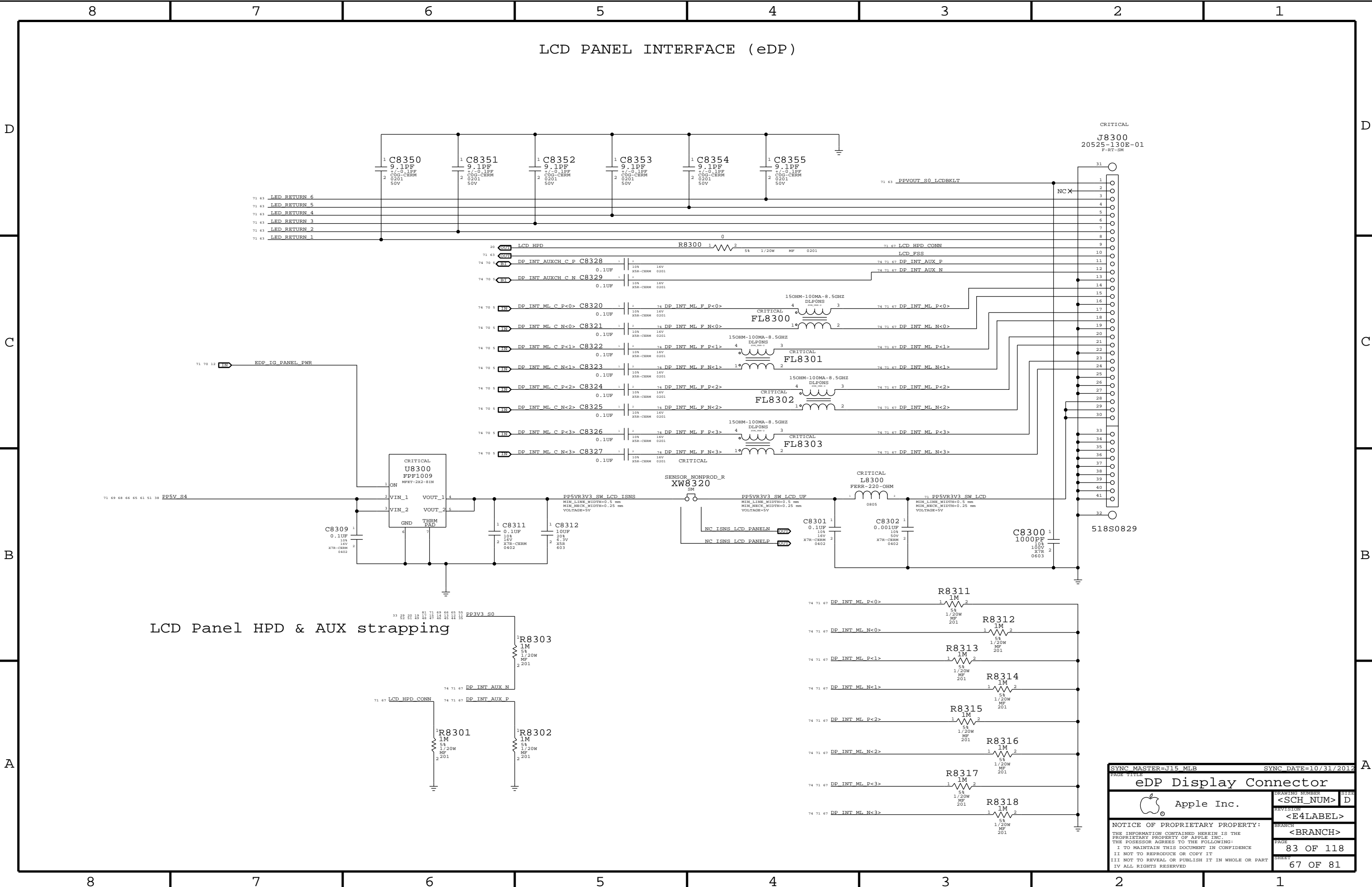
<BRANCH>

PAGE

81 OF 118

SHEET

66 OF 81



LCD Panel HPD & AUX strapping

SYNC MASTER=J15 MLB

SYNC DATE=10/31/2012

eDP Display Connector

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

BRANCH

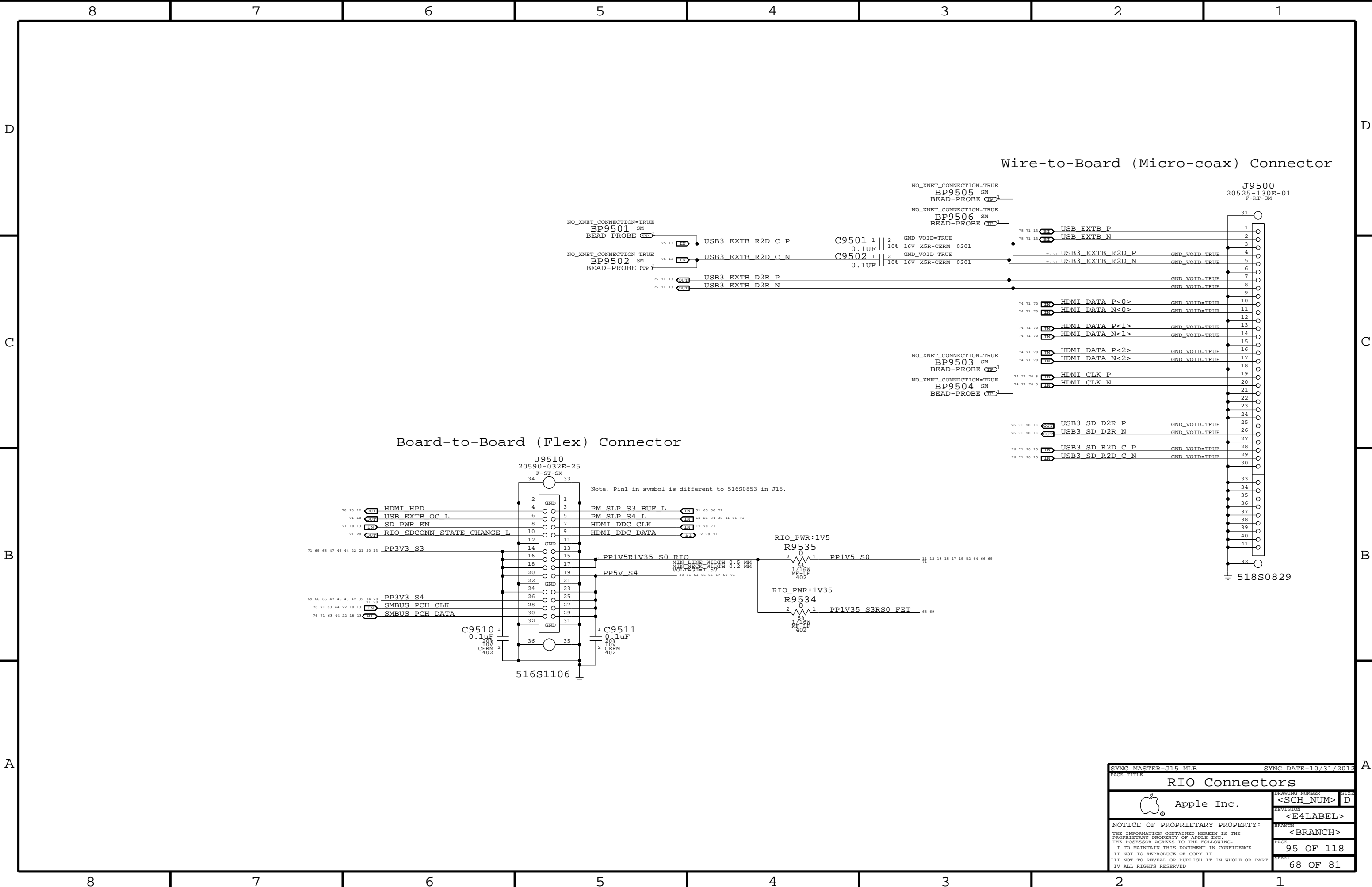
<BRANCH>

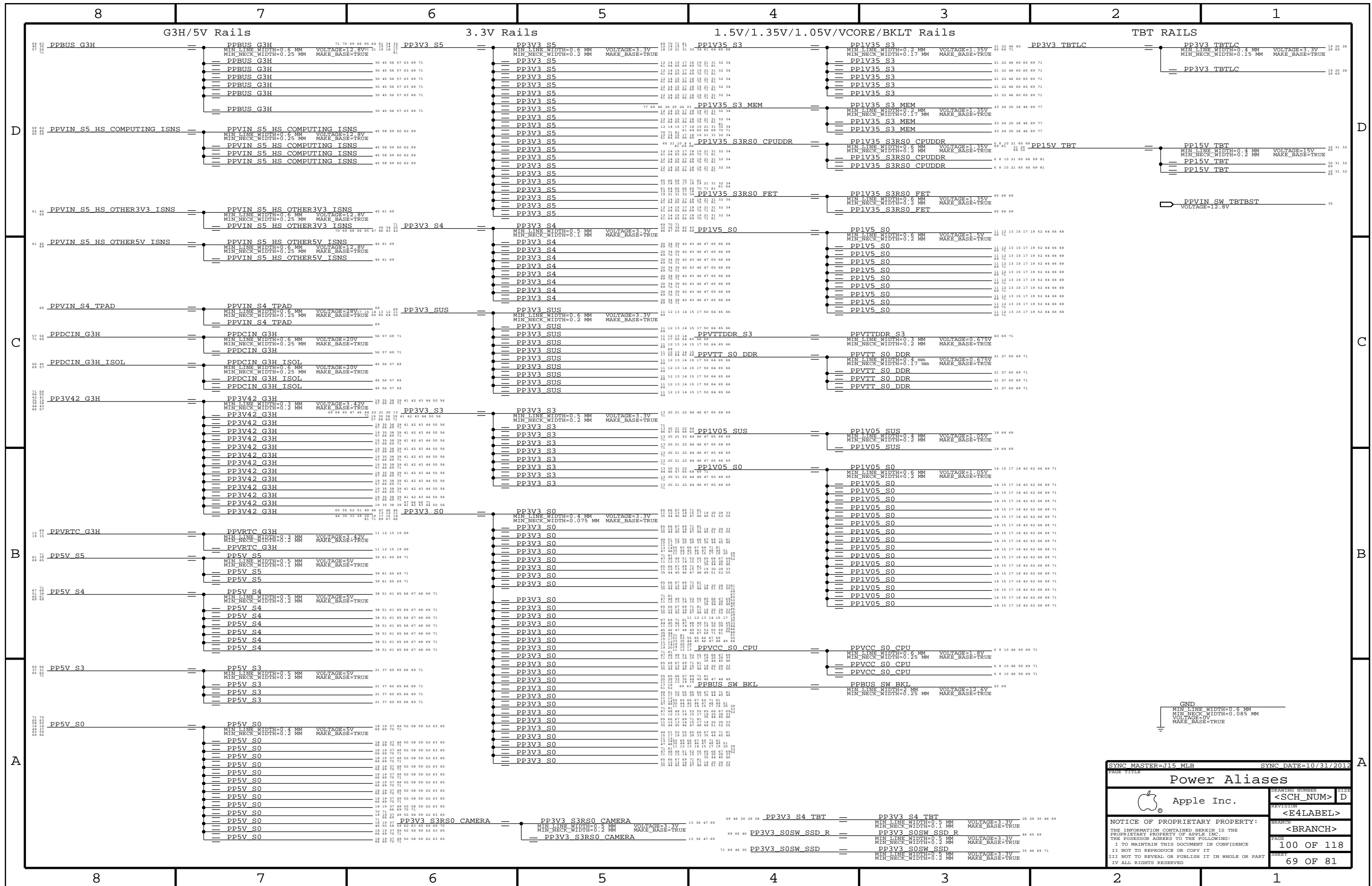
PAGE

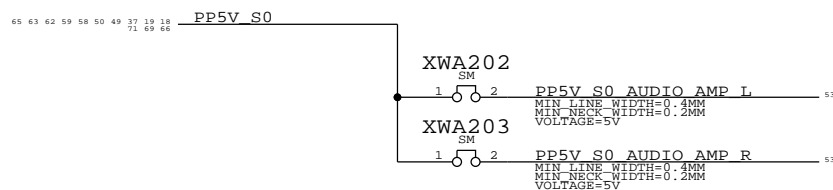
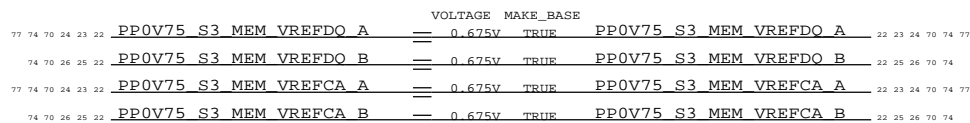
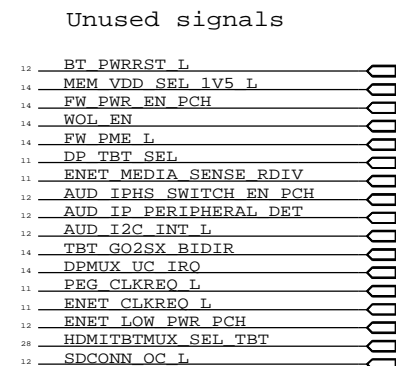
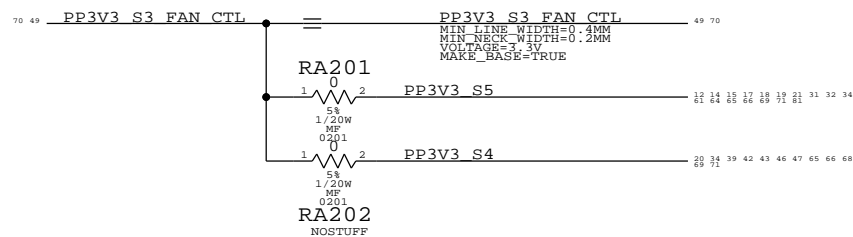
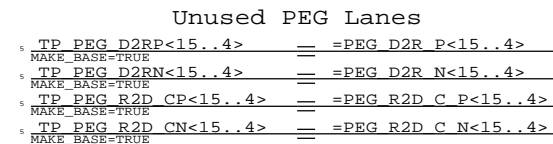
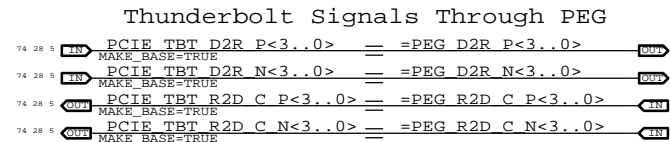
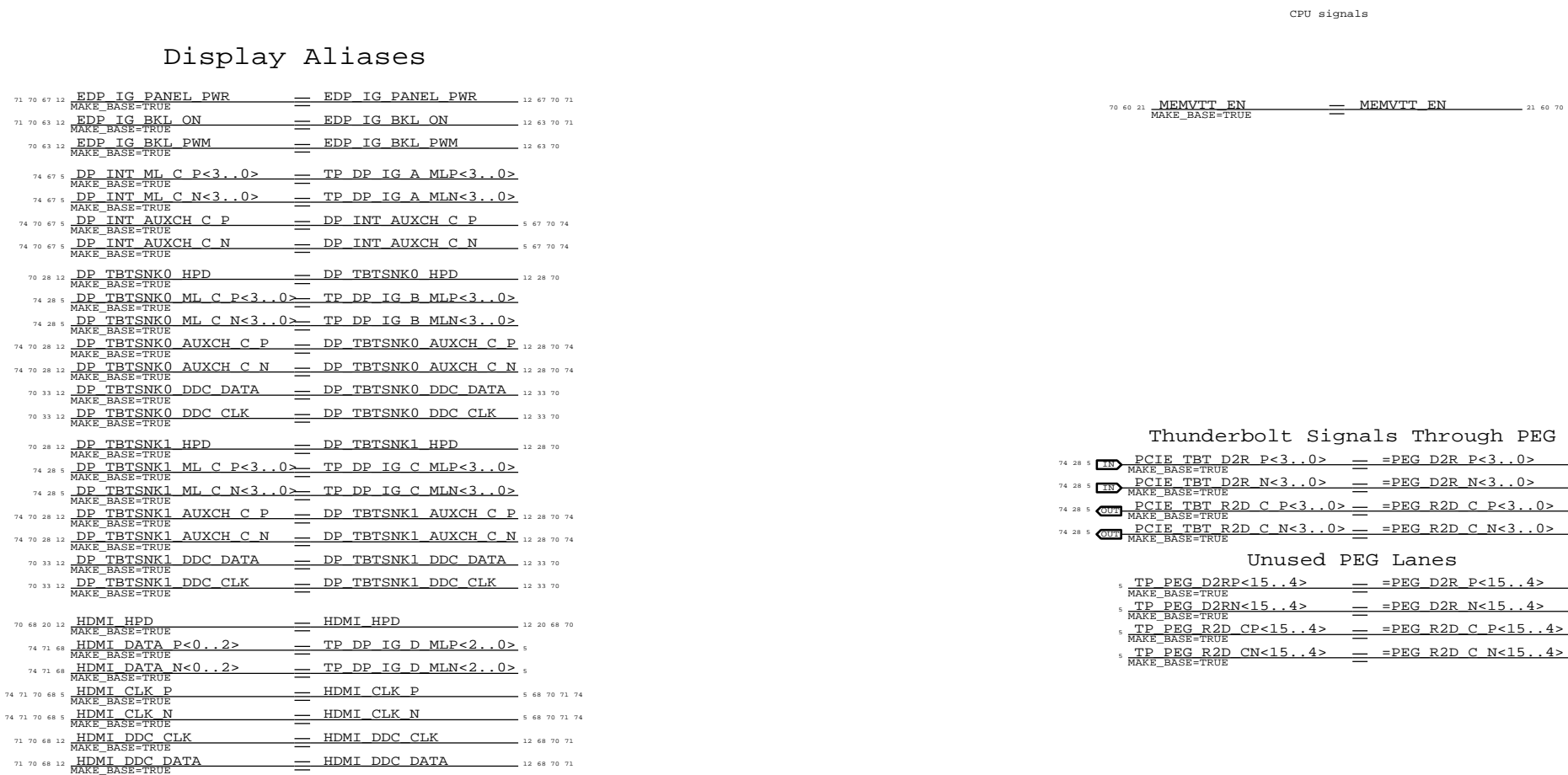
83 OF 118


SHEET

67 OF 81







SYNCH MASTER=J15 MLE		SYNCH DATE=10/31/2012	
PAGE TITLE			
Signal Aliases			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
		SIZE D	
		REVISION <E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		<BRANCH> PAGE 102 OF 118 SHEET 70 OF 81	

Functional Test Points

J3501 - airport	
TRUE AP CLKREQ O L	34
TRUE AP RESET CONN L	34
TRUE PCIE AP D2R PI N	34 76
TRUE PCIE AP D2R PI P	34 76
TRUE PCIE AP R2D N	34 76
TRUE PCIE AP R2D P	34 76
TRUE PCIE CLK100M AP CONN N	34 76
TRUE PCIE CLK100M AP CONN P	34 76
TRUE PCIE WAKE L	12 34 36 76
TRUE PP3V3 S3RS4 BT F	34
TRUE PP3V3 WLAN	34 42
TRUE USB BT CONN N	34 75
TRUE USB BT CONN P	34 75
TRUE WIFI EVENT L	34 41 42
TRUE GND	4X

J4002 - Camera	
TRUE MIPI CLK CONN N	37 79
TRUE MIPI CLK CONN P	37 79
TRUE CAM SENSOR WAKE L CONN	37
TRUE MIPI DATA CONN N	37 79
TRUE MIPI DATA CONN P	37 79
TRUE SMBUS SMC 0 S0 SDA	37 41 44 48 80
TRUE SMBUS SMC 0 S0 SCL	37 41 44 48 80
TRUE I2C CAM SCK	36 37
TRUE I2C CAM SDA	36 37
TRUE PP5V S3RS0 ALSCAM F	37
TRUE GND	

J9500 - rio coax	
TRUE HDMI CLK N	5 68 70 74
TRUE HDMI CLK P	5 68 70 74
TRUE HDMI DATA N<0>	68 70 74
TRUE HDMI DATA N<1>	68 70 74
TRUE HDMI DATA N<2>	68 70 74
TRUE HDMI DATA P<0>	68 70 74
TRUE HDMI DATA P<1>	68 70 74
TRUE HDMI DATA P<2>	68 70 74

TRUE USB3 SD D2R N	13 20 68 76
TRUE USB3 SD D2R P	13 20 68 76
TRUE USB3 SD R2D C N	13 20 68 76
TRUE USB3 SD R2D C P	13 20 68 76
TRUE USB3 EXTB D2R N	13 68 75
TRUE USB3 EXTB D2R P	13 68 75
TRUE USB3 EXTB R2D N	68 75
TRUE USB3 EXTB R2D P	68 75
TRUE USB EXTB N	13 68 75
TRUE USB EXTB P	13 68 75
TRUE GND	19X

J9510 - rio flex	
TRUE SD PWR EN	13 18 68
TRUE PP1V5R1V35 S0 RIO	68
TRUE HDMI DDC CLK	12 68 70
TRUE HDMI DDC DATA	12 68 70
TRUE HDMI HPD L	
TRUE SMBUS PCH CLK	13 18 22 44 63 68 76
TRUE SMBUS PCH DATA	13 18 22 44 63 68 76
TRUE PM SLP S3 BUF L	61 65 66 68
TRUE PM SLP S4 L	12 21 34 38 41 66 68
TRUE PP3V3 S3	3X 13 20 21 22 44 46 47 65 68 69 71
TRUE PP3V3 S4	20 34 39 42 43 46 47 65 66 68
TRUE PP5V S4	5X 38 51 61 65 66 67 68 69
TRUE RIO SDCONN STATE CHANGE L	20 68
TRUE USB EXTB OC L	18 68
TRUE GND	10X

J5150 - hall effect	
TRUE PP3V42 G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE SMC LID R	43
TRUE GND	

J6050 - left fan	
TRUE FAN LT PWM	49
TRUE FAN LT TACH	49
TRUE PP5V S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE GND	5X

J6060 - right fan	
TRUE FAN RT PWM	49
TRUE FAN RT TACH	49
TRUE PP5V S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE GND	5X

J6100 - lpc + spi	
TRUE LPCPLUS GPIO	14 50
TRUE LPCPLUS RESET L	20 50 76
TRUE LPC AD<0>	13 41 50 76
TRUE LPC AD<1>	13 41 50 76
TRUE LPC AD<2>	13 41 50 76
TRUE LPC AD<3>	13 41 50 76
TRUE LPC CLK33M LPCPLUS	19 50 76
TRUE LPC FRAME L	13 41 50 76
TRUE LPC PWRDWN L	12 20 41 50
TRUE LPC SERIRO	13 41 50
TRUE PM CLKRUN L	12 41 50
TRUE PP5V S0	18 19 37 49 50 58 59 62 63 65
TRUE SMC RESET L	41 42 50 57
TRUE SMC ROMBOOT	42 50
TRUE SMC RX L	41 42 50
TRUE SMC TCK	41 42 50
TRUE SMC TDI	41 42 50
TRUE SMC TDO	41 42 50
TRUE SMC TMS	41 42 50
TRUE SMC TX L	41 42 50
TRUE SPIROM USE MLB	14 50
TRUE SPI ALT CLK	50
TRUE SPI ALT CS L	50
TRUE SPI ALT MISO	50
TRUE SPI ALT MOSI	50
TRUE TP SMC MD1	50
TRUE TP SMC TRST L	50
TRUE GND	2X

J4800 - ipd flex	
TRUE Z2 CS L	39
TRUE Z2 MOSI	39
TRUE Z2 MISO	39
TRUE Z2 SCLK	39
TRUE Z2 HOST INTN	39
TRUE Z2 CLKIN	39
TRUE Z2 KEY ACT L	39
TRUE PSOC F CS L	39
TRUE PICKB L	39
TRUE PSOC MOSI	39
TRUE PSOC MISO	39
TRUE PSOC SCLK	39
TRUE SMBUS SMC 2 S3 SCL	39 41 44 80
TRUE SMBUS SMC 2 S3 SDA	39 41 44 80
TRUE SMC LID	39 41 42 43
TRUE SMC T101 COM 1	
TRUE PP3V3 S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE PP5V S5	39 61 65 69 71
TRUE GND	2X

J4813 - keyboard	
TRUE PP3V3 S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE PP3V42 G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE WS CONTROL KBD	39
TRUE WS KBD1	39
TRUE WS KBD10	39
TRUE WS KBD11	39
TRUE WS KBD12	39
TRUE WS KBD13	39
TRUE WS KBD14	39
TRUE WS KBD15 CAP	39
TRUE WS KBD16 NUM	39
TRUE WS KBD17	39
TRUE WS KBD18	39
TRUE WS KBD19	39
TRUE WS KBD2	39
TRUE WS KBD20	39
TRUE WS KBD21	39
TRUE WS KBD22	39
TRUE WS KBD23	39
TRUE WS KBD3	39
TRUE WS KBD4	39
TRUE WS KBD5	39
TRUE WS KBD6	39
TRUE WS KBD7	39
TRUE WS KBD8	39
TRUE WS KBD9	39
TRUE WS KBD ONOFF L	39
TRUE WS LEFT OPTION KBD	39
TRUE WS LEFT SHIFT KBD	39
TRUE GND	2X

J4915 - kbd bklt	
TRUE KBD BKLT RETURN1	2X 40 63
TRUE KBD BKLT RETURN2	2X 40 63
TRUE PPVOUT S0 KBD BKLT	40 63
TRUE GND	4X

J6701 - audio flex	
TRUE AUD HP PORT L	51 55
TRUE AUD HP PORT R	51 55
TRUE AUD SPDIF OUT JACK	
TRUE AUD TIPDET INV	
TRUE AUD TYPEDET	51 55
TRUE AUD CONN MIC XW	4X
TRUE CH HS MIC	
TRUE PP3V3 S0	65 66 67 69 71 81 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE AUD CONN SLEEVE XW	4X 54 55
TRUE US HS MIC	
TRUE GND	2X GND

J6601 - mic	
TRUE DMIC CLK3	52 55
TRUE PP3V3 S0	65 66 67 69 71 81
TRUE DMIC SDA2	55
TRUE DMIC SDA3	52 55
TRUE GND	

J6602 - L speaker	
TRUE SPKRCONN L ID	53 55 81
TRUE SPKRCONN L OUT N	53 55 81
TRUE SPKRCONN L OUT P	53 55 81
TRUE SPKRCONN SL OUT N	53 55 81
TRUE SPKRCONN SL OUT P	53 55 81
TRUE GND	

J6603 - R speaker	
TRUE SPKRCONN R ID	53 55 81
TRUE SPKRCONN R OUT N	53 55 81
TRUE SPKRCONN R OUT P	53 55 81
TRUE SPKRCONN SR OUT N	53 55 81
TRUE SPKRCONN SR OUT P	53 55 81
TRUE GND	

J7000 - DC PWR	
TRUE ADAPTER SENSE	56
TRUE PP20V DCIN FUSE	2X 56
TRUE GND	2X

J7050 - battery	
TRUE PPVBAT G3H CONN	8X 56 57
TRUE SMBUS SMC 5 G3 SCL	41 44 56 57 80
TRUE SMBUS SMC 5 G3 SDA	41 44 56 57 80
TRUE SYS DETECT L	56
TRUE GND	8X

J8300 - eDP	
TRUE DP INT AUX N	67 74
TRUE DP INT AUX P	67 74
TRUE DP INT ML N<0>	67 74
TRUE DP INT ML N<1>	67 74
TRUE DP INT ML N<2>	67 74
TRUE DP INT ML N<3>	67 74
TRUE DP INT ML P<0>	67 74
TRUE DP INT ML P<1>	67 74
TRUE DP INT ML P<2>	67 74
TRUE DP INT ML P<3>	67 74
TRUE LCD FSS	63 67
TRUE LCD HPD CONN	67
TRUE LED RETURN 1	63 67
TRUE LED RETURN 2	63 67
TRUE LED RETURN 3	63 67
TRUE LED RETURN 4	63 67
TRUE LED RETURN 5	63 67
TRUE LED RETURN 6	63 67
TRUE PP5VR3V3 SW LCD	3X 67
TRUE PPVOUT S0 LCDBKLT	63 67
TRUE GND	16X

Power Rails	
TRUE PM SLP S3 L	12 21 41 66
TRUE PPVTT S0 DDR	21 27 60 69
TRUE PP3V3 S0	65 66 67 69 71 81 19 20 29 33 35 44 45 46 47 48 49 51 52 55 57 60 65 66 69
TRUE PP3V3 S3	71 20 21 22 44 46 47 65 68 69
TRUE PP3V3 S5	22 24 25 26 28 30 31 32 34
TRUE PP3V3 S5 AVREF SMC	41 42
TRUE PP3V42 G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE PP5V S0	18 19 37 49 50 58 59 62 63 65
TRUE PP5V S3	21 37 60 65 66 69
TRUE PP5V S5	39 61 65 69 71
TRUE PPBUS G3H	30 45 56 57 63 69
TRUE PPDCIN G3H	56 57 69
TRUE PPVCC S0 CPU	6 8 10 46 59 69
TRUE PPVTDDR S3	40 69
TRUE PP3V3 S0SW SSD	35 46 69
TRUE PP1V5 S0	65 12 13 15 17 19 52 64 66 68
TRUE PP1V35 S3	21 22 46 60 65 69

XDP	
TRUE XDP CPU TCK	6 18 74
TRUE XDP PCH TCK	11 18
TRUE XDP CPU TDI	6 18 74
TRUE XDP CPU TDO	6 18 74
TRUE XDP CPUPCH TRST L	6 18 74
TRUE XDP CPU TMS	6 18 74
TRUE XDP PCH TMS	11 18
TRUE XDP PCH TDI	11 18
TRUE XDP PCH TDO	11 18
TRUE XDP CPU FREQ L	6 18 74
TRUE XDP CPU PRDY L	6 18 74
TRUE PM RSMRST L	12 66 76
TRUE PM PCH PWROK	12 19 76
TRUE PM SYSRST L	12 19 41 76
TRUE CPU CFG<3>	6 18 74
TRUE PP1V05 S0	14 15 17 18 42 62 66 69
TRUE GND	2X GND

Power Sequence	
TRUE SMC ONOFF L	39 41 42
TRUE PM DSW PWRGD	12 41 76
TRUE ALL SYS PWRGD	18 19 41 58 66
TRUE PM PCH SYS PWROK	12 18 19 41 76
TRUE PLT RESET L	12 18 20 21
TRUE EDP IG PANEL PWR	12 67 70
TRUE EDP IG BKL ON	12 63 70

SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE		DRAWING NUMBER	
Functional Test Points		<SCH_NUM> D	
Apple Inc.		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		<BRANCH>	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		PAGE	
II NOT TO REPRODUCE OR COPY IT		104 OF 118	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET	
IV ALL RIGHTS RESERVED		71 OF 81	

8	7	6	5	4	3	2	1
NC_NO_TESTS							
PCH				Thunderbolt		PLACEABLE BEAD-PROBES FOR TBT	
NO_TEST MAKE_BASE				NO_TEST MAKE_BASE			
72 13	NC_USB3_SPARE_D2RN	==	TRUE TRUE	NC_USB3_SPARE_D2RN	13 72	72 28	NC_TBT_XTAL25OUT
72 13	NC_USB3_SPARE_D2RP	==	TRUE TRUE	NC_USB3_SPARE_D2RP	13 72		
72 13	NC_USB3_SPARE_R2D_CN	==	TRUE TRUE	NC_USB3_SPARE_R2D_CN	13 72		
72 13	NC_USB3_SPARE_R2D_CP	==	TRUE TRUE	NC_USB3_SPARE_R2D_CP	13 72		
75 72 13	NC_USB3_EXTC_D2RN	==	TRUE TRUE	NC_USB3_EXTC_D2RN	13 72 75		
75 72 13	NC_USB3_EXTC_D2RP	==	TRUE TRUE	NC_USB3_EXTC_D2RP	13 72 75		
75 72 13	NC_USB3_EXTC_R2D_CN	==	TRUE TRUE	NC_USB3_EXTC_R2D_CN	13 72 75		
75 72 13	NC_USB3_EXTC_R2D_CP	==	TRUE TRUE	NC_USB3_EXTC_R2D_CP	13 72 75		
75 72 13	NC_USB3_EXTD_D2RN	==	TRUE TRUE	NC_USB3_EXTD_D2RN	13 72 75		
75 72 13	NC_USB3_EXTD_D2RP	==	TRUE TRUE	NC_USB3_EXTD_D2RP	13 72 75		
75 72 13	NC_USB3_EXTD_R2D_CN	==	TRUE TRUE	NC_USB3_EXTD_R2D_CN	13 72 75		
75 72 13	NC_USB3_EXTD_R2D_CP	==	TRUE TRUE	NC_USB3_EXTD_R2D_CP	13 72 75		
72	NC_PCIE_ENET_D2RN	==	TRUE TRUE	NC_PCIE_ENET_D2RN	72		
72	NC_PCIE_ENET_D2RP	==	TRUE TRUE	NC_PCIE_ENET_D2RP	72		
72	NC_PCIE_ENET_R2D_CN	==	TRUE TRUE	NC_PCIE_ENET_R2D_CN	72		
72	NC_PCIE_ENET_R2D_CP	==	TRUE TRUE	NC_PCIE_ENET_R2D_CP	72		
75 72 11	NC_SATA_A_D2RN	==	TRUE TRUE	NC_SATA_A_D2RN	11 72 75		
75 72 11	NC_SATA_A_D2RP	==	TRUE TRUE	NC_SATA_A_D2RP	11 72 75		
75 72 11	NC_SATA_A_R2D_CN	==	TRUE TRUE	NC_SATA_A_R2D_CN	11 72 75		
75 72 11	NC_SATA_A_R2D_CP	==	TRUE TRUE	NC_SATA_A_R2D_CP	11 72 75		
75 72 11	NC_SATA_B_D2RN	==	TRUE TRUE	NC_SATA_B_D2RN	11 72 75		
75 72 11	NC_SATA_B_D2RP	==	TRUE TRUE	NC_SATA_B_D2RP	11 72 75		
75 72 11	NC_SATA_B_R2D_CN	==	TRUE TRUE	NC_SATA_B_R2D_CN	11 72 75		
75 72 11	NC_SATA_B_R2D_CP	==	TRUE TRUE	NC_SATA_B_R2D_CP	11 72 75		
75 72 11	NC_SATA_ODD_D2RN	==	TRUE TRUE	NC_SATA_ODD_D2RN	11 72 75		
72 11	NC_SATA_ODD_D2RP	==	TRUE TRUE	NC_SATA_ODD_D2RP	11 72 75		
72 11	NC_SATA_ODD_R2D_CN	==	TRUE TRUE	NC_SATA_ODD_R2D_CN	11 72 75		
72 11	NC_SATA_ODD_R2D_CP	==	TRUE TRUE	NC_SATA_ODD_R2D_CP	11 72 75		
72 11	NC_SATA_D_D2RN	==	TRUE TRUE	NC_SATA_D_D2RN	11 72 75		
72 11	NC_SATA_D_D2RP	==	TRUE TRUE	NC_SATA_D_D2RP	11 72 75		
72 11	NC_SATA_D_R2D_CN	==	TRUE TRUE	NC_SATA_D_R2D_CN	11 72 75		
72 11	NC_SATA_D_R2D_CP	==	TRUE TRUE	NC_SATA_D_R2D_CP	11 72 75		
72 11	NC_SATA_F_D2RN	==	TRUE TRUE	NC_SATA_F_D2RN	11 72 75		
72 11	NC_SATA_F_D2RP	==	TRUE TRUE	NC_SATA_F_D2RP	11 72 75		
72 11	NC_SATA_F_R2D_CN	==	TRUE TRUE	NC_SATA_F_R2D_CN	11 72 75		
72 11	NC_SATA_F_R2D_CP	==	TRUE TRUE	NC_SATA_F_R2D_CP	11 72 75		
75 72 13	NC_USB_EXTCN	==	TRUE TRUE	NC_USB_EXTCN	13 72 75		
75 72 13	NC_USB_EXTCP	==	TRUE TRUE	NC_USB_EXTCP	13 72 75		
75 72 13	NC_USB_SDN	==	TRUE TRUE	NC_USB_SDN	13 72 75		
75 72 13	NC_USB_SDP	==	TRUE TRUE	NC_USB_SDP	13 72 75		
72 13	NC_USB_WLANN	==	TRUE TRUE	NC_USB_WLANN	72		
72 13	NC_USB_WLANP	==	TRUE TRUE	NC_USB_WLANP	72		
75 72 13	NC_USB_6N	==	TRUE TRUE	NC_USB_6N	13 72 75		
75 72 13	NC_USB_6P	==	TRUE TRUE	NC_USB_6P	13 72 75		
75 72 13	NC_USB_7N	==	TRUE TRUE	NC_USB_7N	13 72 75		
75 72 13	NC_USB_7P	==	TRUE TRUE	NC_USB_7P	13 72 75		
75 72 13	NC_USB_EXTDN	==	TRUE TRUE	NC_USB_EXTDN	13 72 75		
75 72 13	NC_USB_EXTDP	==	TRUE TRUE	NC_USB_EXTDP	13 72 75		
72 13	NC_USB_PSOEN	==	TRUE TRUE	NC_USB_PSOEN	72		
72 13	NC_USB_PSOCP	==	TRUE TRUE	NC_USB_PSOCP	72		
75 72 13	NC_USB_IRN	==	TRUE TRUE	NC_USB_IRN	13 72 75		
75 72 13	NC_USB_IRP	==	TRUE TRUE	NC_USB_IRP	13 72 75		
74 72 11	NC_ITPXDP_CLK100MN	==	TRUE TRUE	NC_ITPXDP_CLK100MN	11 72 74		
74 72 11	NC_ITPXDP_CLK100MP	==	TRUE TRUE	NC_ITPXDP_CLK100MP	11 72 74		
72 12	NC_PCI_PME_L	==	TRUE TRUE	NC_PCI_PME_L	72		
72 11	NC_PCI_CLK33M_OUT2	==	TRUE TRUE	NC_PCI_CLK33M_OUT2	72		
72 11	NC_PCI_CLK33M_OUT3	==	TRUE TRUE	NC_PCI_CLK33M_OUT3	72		
72 11	NC_HDA_SDIN1	==	TRUE TRUE	NC_HDA_SDIN1	72		
72 11	NC_HDA_SDIN2	==	TRUE TRUE	NC_HDA_SDIN2	72		
72 11	NC_HDA_SDIN3	==	TRUE TRUE	NC_HDA_SDIN3	72		
72 13	NC_LPC_DREQ0_L	==	TRUE TRUE	NC_LPC_DREQ0_L	13 72		
72 13	NC_CLINK_CLK	==	TRUE TRUE	NC_CLINK_CLK	13 72		
72 13	NC_CLINK_DATA	==	TRUE TRUE	NC_CLINK_DATA	13 72		
72 13	NC_CLINK_RESET_L	==	TRUE TRUE	NC_CLINK_RESET_L	13 72		
75 72	NC_USB_S MCP	==	TRUE TRUE	NC_USB_S MCP	72 75		
75 72	NC_USB_S MCN	==	TRUE TRUE	NC_USB_S MCN	72 75		
72	NC_SMC_INTERFACE_2	==	TRUE TRUE	NC_SMC_INTERFACE_2	72		
</							

J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA, P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules


Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNCH MASTER=SIDLE J45		SYNCH DATE=12/10/2012	
PAGE TITLE			
PCB Rule Definitions			
 Apple Inc.	DRAWING NUMBER	SIZE	
	<SCH_NUM>		D
	REVISION		
	<E4LABEL>		
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
BRANCH		<BRANCH>	
PAGE		110 OF 118	
SHEET		73 OF 81	

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	20 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?	DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?	DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2N2S	*	=6X_DIELECTRIC	?	DMICKLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2S2N	*	=3X_DIELECTRIC	?	DMICKLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICKLK2OTHER	*	=4X_DIELECTRIC	?	DMICKLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICKLK2N2S
CLK_DMI	DMI_S2N	*	DMICKLK2S2N
CLK_DMI	*	*	DMICKLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?	PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?	PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?	PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?	PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?	DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?	HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?	HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?	HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDs intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDs TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0> 5 12 72
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0> 5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0> 5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0> 5 12 72
FDI_INT	CPU_50S	CPU_AGTL	FDI INT 5 12
FDI_CSVMC	CPU_50S	CPU_AGTL	FDI CSVMC 5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI CLK100M CPU P 4 11
DMI_CLK	CPU_85D	CLK_DMI	DMI CLK100M CPU N 4 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU CLK135M DPLLREF N 6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU CLK135M DPLLREF P 6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU CLK135M DPLLSS N 6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU CLK135M DPLLSS P 6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU EDP RCOMP 5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU PEG RCOMP 5
CPU_CFG	CPU_45S	CPU_ITP	CPU CFG<19..0> 6 18 71
XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	NC ITPXDP CLK100MP 11 72
XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	NC ITPXDP CLK100MN 11 72
XDP_TDI	CPU_45S	CPU_ITP	XDP CPU TDI 6 18 71
XDP_TDO	CPU_45S	CPU_ITP	XDP CPU TDO 6 18 71
XDP_TMS	CPU_45S	CPU_ITP	XDP CPU TMS 6 18 71
XDP_TCK	CPU_45S	CPU_ITP	XDP CPU TCK 6 18 71
XDP_TRST_L	CPU_45S	CPU_ITP	XDP CRUPCH TRST L 6 18 71
XDP_BPM	CPU_45S	CPU_ITP	XDP BPM L<3..0> 6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP BPM L<7..4> 6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP DBRESET L 6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP CPU PRDY L 6 18 71
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP CPU PREQ L 6 18 71
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU CATERR L 6 41
CPU_PECI	CPU_45S	CPU_VID	CPU Peci 6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU PROCHOT L 6 41 42 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU PWRGD 6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_SMIL	PM THRMTRIP L 6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM MEM PWRGD 6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM SYNC 6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP<2..0> 6
CPU_VID	CPU_45S	CPU_VID	CPU VIDSOUT 8 58
CPU_VID	CPU_45S	CPU_VID	CPU VIDCLK 8 58
CPU_VID	CPU_45S	CPU_VID	CPU VIDALERT L 8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P 8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N 9 58
CPU_MEM_VREF		CPU_VREF	CPU DIMMA VREFDQ 7 22
CPU_MEM_VREF		CPU_VREF	CPU DIMMB VREFDQ 7 22
CPU_MEM_VREF		MEM_PWR	PP0V75 S3 MEM VREFDQ A 22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75 S3 MEM VREFDQ B 22 25 26 70
CPU_MEM_VREF		MEM_PWR	PP0V75 S3 MEM VREFCA A 22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75 S3 MEM VREFCA B 22 25 26 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R P<3..0> 5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R N<3..0> 5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R C P<3..0> 28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D P<3..0> 28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D N<3..0> 28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D C P<3..0> 5 28 70
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D C N<3..0> 5 28 70

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML C P<3..0> 5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML C N<3..0> 5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML P<3..0> 67 71 74
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML N<3..0> 67 71 74
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML F N<3..0> 67
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML F P<3..0> 67
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML P<3..0> 67 71 74
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML N<3..0> 67 71 74
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH C P 5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH C N 5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUX P 67 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUX N 67 71

DP / HDMI NET PROPERTIES


ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI DATA P<2..0> 68 70 71
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI DATA N<2..0> 68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI CLK P 5 68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI CLK N 5 68 70 71
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0> 5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0> 5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0> 28
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0> 28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0> 5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0> 5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0> 28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0> 28
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH P 28
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH N 28
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH C P 12 28 70
TBTSNK0_AUXCH	DP_85D		DP TBTSNK0 AUXCH C N 12 28 70
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH P 28
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH N 28
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH C P 12 28 70
TBTSNK1_AUXCH	DP_85D		DP TBTSNK1 AUXCH C N 12 28 70

SYNC MASTER=SIDLE J45

SYNC DATE=12/10/2012

PAGE TITLE

CPU Constraints

 Apple Inc.

DRAWING NUMBER
<SCH_NUM> D

REVISION
<E4LABEL>

BRANCH
<BRANCH>

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE
111 OF 118

SHEET
74 OF 81

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4X_DIELECTRIC	?
CLK_25M	*	=5X_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
<div></div>	SATA_R5D	SATA_R2D	NC SATA A R2D CP 11 72
<div></div>	SATA_85D	SATA_R2D	NC SATA A R2D CN 11 72
<div></div>	SATA_85D	SATA_D2R	NC SATA A D2RP 11 72
<div></div>	SATA_85D	SATA_D2R	NC SATA A D2RN 11 72
<div></div>	SATA_85D	SATA_R2D	NC SATA B R2D CP 11 72
<div></div>	SATA_85D	SATA_R2D	NC SATA B R2D CN 11 72
<div></div>	SATA_85D	SATA_D2R	NC SATA B D2RP 11 72
<div></div>	SATA_85D	SATA_D2R	NC SATA B D2RN 11 72
<div></div>			
<div></div>	PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP PCH SATA RCOMP 11
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_P 13 38
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_N 13 38
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_MUXED_P 38
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_MUXED_N 38
<div></div>	USB_EXTN	USB_85D	USB USB_LT1_P 38
<div></div>	USB_EXTN	USB_85D	USB USB_LT1_N 38
<div></div>			
<div></div>	USB_NC	USB_85D	NC USB_EXTCP 13 72
<div></div>	USB_NC	USB_85D	NC USB_EXTCN 13 72
<div></div>	USB_NC	USB_85D	NC USB_SDP 13 72
<div></div>	USB_NC	USB_85D	NC USB_SDN 13 72
<div></div>	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L 38 41 42
<div></div>	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L 38 41 42
<div></div>	USB_SMC	USB_85D	NC USB_SMCP 72
<div></div>	USB_SMC	USB_85D	NC USB_SMCN 72
<div></div>			
<div></div>	USB_NC	USB_85D	NC USB_6P 13 72
<div></div>	USB_NC	USB_85D	NC USB_6N 13 72
<div></div>	USB_NC	USB_85D	NC USB_7P 13 72
<div></div>	USB_NC	USB_85D	NC USB_7N 13 72
<div></div>	USB_EXTB	USB_85D	USB USB_EXTB_P 13 68 71
<div></div>	USB_EXTB	USB_85D	USB USB_EXTB_N 13 68 71
<div></div>	USB_NC	USB_85D	NC USB_EXTRDP 13 72
<div></div>	USB_NC	USB_85D	NC USB_EXTRDN 13 72
<div></div>	USB_BT	USB_85D	USB BT_P 13 34
<div></div>	USB_BT	USB_85D	USB BT_N 13 34
<div></div>	USB_85D	USB	USB_BT_CONN_P 34 71
<div></div>	USB_85D	USB	USB_BT_CONN_N 34 71
<div></div>	USB_NC	USB_85D	NC USB_IRP 13 72
<div></div>	USB_NC	USB_85D	NC USB_IRN 13 72
<div></div>	USB_TPAD	USB_85D	USB USB_TPAD_P 13 39
<div></div>	USB_TPAD	USB_85D	USB USB_TPAD_N 13 39
<div></div>	USB_85D	USB	USB USB_TPAD_R_P 39
<div></div>	USB_85D	USB	USB USB_TPAD_R_N 39
<div></div>	PCH_USB_RBIAS	PCH_USB_RBIAS	USB USB_RBIAS 13
<div></div>			
<div></div>	USB3_EXTN_RX	USB_85D	USB3 USB3_EXTN_D2R_P 13 38
<div></div>	USB3_EXTN_RX	USB_85D	USB3 USB3_EXTN_D2R_N 13 38
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTN_D2R_C_P 13 38
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTN_D2R_C_N 13 38
<div></div>	USB3_EXTN_TX	USB_85D	USB3 USB3_EXTN_R2D_P 38
<div></div>	USB3_EXTN_TX	USB_85D	USB3 USB3_EXTN_R2D_N 38
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTN_R2D_C_P 13 38
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTN_R2D_C_N 13 38
<div></div>	USB3_EXTB_RX	USB_85D	USB3 USB3_EXTB_D2R_P 13 68 71
<div></div>	USB3_EXTB_RX	USB_85D	USB3 USB3_EXTB_D2R_N 13 68 71
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTB_D2R_C_P 68 71
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTB_D2R_C_N 68 71
<div></div>	USB3_EXTB_TX	USB_85D	USB3 USB3_EXTB_R2D_P 13 68
<div></div>	USB3_EXTB_TX	USB_85D	USB3 USB3_EXTB_R2D_N 13 68
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTB_R2D_C_P 13 68
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTB_R2D_C_N 13 72
<div></div>	NC_USB3	USB_85D	NC USB3_EXTN_D2RP 13 72
<div></div>	NC_USB3	USB_85D	NC USB3_EXTN_D2RN 13 72
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTN_R2D_CP 13 72
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTN_R2D_CN 13 72
<div></div>	NC_USB3	USB_85D	NC USB3_EXTD_D2RP 13 72
<div></div>	NC_USB3	USB_85D	NC USB3_EXTD_D2RN 13 72
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTD_R2D_CP 13 72
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTD_R2D_CN 13 72

Clock Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
<div></div>	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW SYSCLK_CLK32K_RTC 11 19
<div></div>	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M SYSCLK_CLK25M_SB 11 19
<div></div>	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M SYSCLK_CLK25M_CAMERA 19 37
<div></div>	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M SYSCLK_CLK25M_TBT 19 28
<div></div>		CLK_25M_45S	CLK_25M SYSCLK_CLK25M_TBT_R 28

SYNC MASTER=SIDLE_J45

SYNC DATE=12/10/2012

PCH Constraints 1

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

<SCH_NUM> D

REVISION

<E4LABEL>

BRANCH

<BRANCH>

PAGE

112 OF 118

SHEET

75 OF 81

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?	PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PC1E_8SD	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PC1E_8SD	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL		NET_TYPE		SPACING	
	LPC_AD	LPC_45S	LPC		LPC AD<3..0>	13	41 50 71
	LPC_FRAME_L	LPC_45S	LPC		LPC FRAME L	13	41 50 71
	LPC_RESET_L	LPC_45S	LPC		LPCPLUS RESET L	20	50 71
	SMBUS_PCH_CLK	SMR_45S	SMR		SMBUS PCH CLK	13	18 22 44 63 68 71
	SMBUS_PCH_DATA	SMR_45S	SMR		SMBUS PCH DATA	13	18 22 44 63 68 71
	SMBUS_PCH_0_CLK	SMR_45S	SMR		SML PCH 0 CLK	13	44
	SMBUS_PCH_0_DATA	SMR_45S	SMR		SML PCH 0 DATA	13	44
	SMBUS_PCH_1_CLK	SMR_45S	SMR		SML PCH 1 CLK	13	44
	SMBUS_PCH_1_DATA	SMR_45S	SMR		SML PCH 1 DATA	13	44
	HDA_BIT_CLK	HDA_45S	HDA		HDA BIT CLK	11	52
	HDA_BIT_CLK_R	HDA_45S	HDA		HDA BIT CLK R	11	
	HDA_SYNC	HDA_45S	HDA		HDA SYNC	11	52
	HDA_SYNC_R	HDA_45S	HDA		HDA SYNC R	11	
	HDA_RST_R_L	HDA_45S	HDA		HDA RST R L	11	
	HDA_RST_L	HDA_45S	HDA		HDA RST L	11	52
	HDA_SDIO0	HDA_45S	HDA		HDA SDIO0	11	52
	HDA_SDIO0_R	HDA_45S	HDA		CS4208 HDA SDOUT0 R	52	
	HDA_SDOUT	HDA_45S	HDA		HDA SDOUT	11	52
	HDA_SDOUT_R	HDA_45S	HDA		HDA SDOUT R	11	19
	SPT_CLK	SPT_45S	SPT		SPI CLK R	13	50
	SPT_CLK	SPT_45S	SPT		SPI CLK	50	
	SPT_MOST	SPT_45S	SPT		SPI MOST R	13	50
	SPT_MOST	SPT_45S	SPT		SPI MOSI	50	
	SPT_MISO	SPT_45S	SPT		SPI MISO	13	50
	SPT_CS0	SPT_45S	SPT		SPI CS0 R L	13	50
	SPT_CS0	SPT_45S	SPT		SPI CS0 L	50	
	USB3_SD_R2D	USB3_85D	USB3_R2D		USB3 SD R2D C P	13	20 68 71
	USB3_SD_R2D	USB3_85D	USB3_R2D		USB3 SD R2D C N	13	20 68 71
	USB3_SD_D2R	USB3_85D	USB3_D2R		USB3 SD D2R P	13	20 68 71
	USB3_SD_D2R	USB3_85D	USB3_D2R		USB3 SD D2R N	13	20 68 71
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D		PCIE AP R2D P	34	71
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D		PCIE AP R2D N	34	71
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D		PCIE AP R2D C P	13	34
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D		PCIE AP R2D C N	13	34
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D		PCIE AP R2D PI P	34	
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D		PCIE AP R2D PI N	34	
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R		PCIE AP D2R P	13	34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R		PCIE AP D2R N	13	34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R		PCIE AP D2R PI P	34	71
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R		PCIE AP D2R PI N	34	71
	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D		PCIE CAMERA R2D P	36	37
	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D		PCIE CAMERA R2D N	36	37
	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D		PCIE CAMERA R2D C P	13	37
	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D		PCIE CAMERA R2D C N	13	37
	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R		PCIE CAMERA D2R P	13	37
	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R		PCIE CAMERA D2R N	13	37
	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R		PCIE CAMERA D2R C P	36	37
	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R		PCIE CAMERA D2R C N	36	37
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC		LPC CLK33M SMC R	11	19
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC		LPC CLK33M SMC	19	41
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC		LPC CLK33M LPCPLUS	19	50 71
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC		LPC CLK33M LPCPLUS R	11	19

PCH Net Properties

NET_NAME		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCB_PM_NET	PCB_45S	PCB_SE	PCB_INTRUDER_L	11
PCB_PM_NET	PCB_45S	PCB_SE	PCB_INTVRMEN_L	11
PCB_PM_NET	PCB_45S	PCB_SE	PCB_DSIVRMEN	11
PCB_PM_NET	PCB_45S	PCB_SE	PCB_SRTCRST_L	12
PCB_PM_NET	PCB_45S	PCB_SE	PM_RSMRST_L	12 66 71
PCB_PM_NET	PCB_45S	PCB_SE	PM_SYSRST_L	12 19 41 71
PCB_PM_NET	PCB_45S	PCB_SE	PM_PCH_PWR0K	12 19 71 76
PCB_PM_NET	PCB_45S	PCB_SE	PM_PCH_PWR0K	12 19 71 76
PCB_PM_NET	PCB_45S	PCB_SE	PM_DSW_PWRGD	12 41 71
PCB_PM_NET	PCB_45S	PCB_SE	PM_PCH_SYS_PWR0K	12 18 19 41 71
PCB_PM_NET	PCB_45S	PCB_SE	PM_PWRBTN_L	12 18 41
PCB_PM_NET	PCB_45S	PCB_SE	PM_THRMTRIP_L_R	14 42
PCB_PCIE_WAKE	PCB_45S	PCB_SE	PCIE_WAKE_L	12 14 36 71
PCB_PM_NET	PCB_45S	PCB_SE	PCB_RCIN_L	14
PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD D2R P<3..0>	13 35
PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD D2R N<3..0>	13 35
PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD R2D C P<3..0>	13 35
PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD R2D C N<3..0>	13 35
	PCIE_85D	PCIE_R2D	PCIE_SSD R2D P<3..0>	35
	PCIE_85D	PCIE_R2D	PCIE_SSD R2D N<3..0>	35

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM A CLK P<0>	7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM A CLK N<0>	7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM A CLK P<1>	7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM A CLK N<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM A CKE<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM A CKE<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM A CS L<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM A CS L<1>	7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM A ODT<0>	7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM A ODT<1>	7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM A DQ<7..0>	7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM A DQ<15..8>	7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM A DQ<23..16>	7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM A DQ<31..24>	7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM A DQ<39..32>	7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM A DQ<47..40>	7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM A DQ<55..48>	7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM A DQ<63..56>	7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM A DQS P<0>	7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM A DQS N<0>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM A DQS P<1>	7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM A DQS N<1>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM A DQS P<2>	7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM A DQS N<2>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM A DQS P<3>	7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM A DQS N<3>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM A DQS P<4>	7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM A DQS N<4>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM A DQS P<5>	7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM A DQS N<5>	7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM A DQS P<6>	7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM A DQS N<6>	7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM A DQS P<7>	7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM A DQS N<7>	7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM B CLK P<0>	7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM B CLK N<0>	7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM B CLK P<1>	7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM B CLK N<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM B CKE<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM B CKE<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM B CS L<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM B CS L<1>	7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM B ODT<0>	7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM B ODT<1>	7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM B DQ<7..0>	7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM B DQ<15..8>	7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM B DQ<23..16>	7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM B DQ<31..24>	7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM B DQ<39..32>	7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM B DQ<47..40>	7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM B DQ<55..48>	7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM B DQ<63..56>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM B DQS P<0>	7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM B DQS N<0>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM B DQS P<1>	7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM B DQS N<1>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM B DQS P<2>	7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM B DQS N<2>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM B DQS P<3>	7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM B DQS N<3>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM B DQS P<4>	7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM B DQS N<4>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM B DQS P<5>	7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM B DQS N<5>	7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM B DQS P<6>	7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM B DQS N<6>	7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM B DQS P<7>	7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM B DQS N<7>	7 25 26
		MEM_PWR	PP0V75_S3 MEM VREFD0 A	22 23 24 70 74
		MEM_PWR	PP0V75_S3 MEM VREFCA A	22 23 24 70 74
		MEM_PWR	PP1V35_S3 MEM	23 24 25 26 46 69

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
Memory Constraints			
 Apple Inc.	DRAWING NUMBER	SIZE	
	<SCH_NUM>	D	
	REVISION		
	<E4LABEL>		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH		
	<BRANCH>		
	PAGE	114 OF 118	
	SHEET	77 OF 81	

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3x_DIELECTRIC	?
TBTDP_TXRX	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C P<1..0>	28 31 72
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C N<1..0>	28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D P<1..0>	31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D N<1..0>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML N<1>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R P<0>	28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R N<0>	28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R P<1>	28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R N<1>	28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC P	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC N	31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C P	28 31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C N	28 31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH P	31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH N	31


TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C P<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C N<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D P<1..0>	32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D N<1..0>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML N<1>	32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3>	28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3>	28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<3>	32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<3>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R P<0>	28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R N<0>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R P<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R N<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC P	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC N	32
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH C P	28 32
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH C N	28 32
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH P	32
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH N	32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>	
	DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>	
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P	
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT SPI CLK	28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI	28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT SPI MISO	28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT SPI CS L	28

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
Thunderbolt Constraints			
 Apple Inc.	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION		
	<E4LABEL>		
	BRANCH		
	<BRANCH>		
	PAGE		
	115 OF 118		
	SHEET		
	78 OF 81		

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

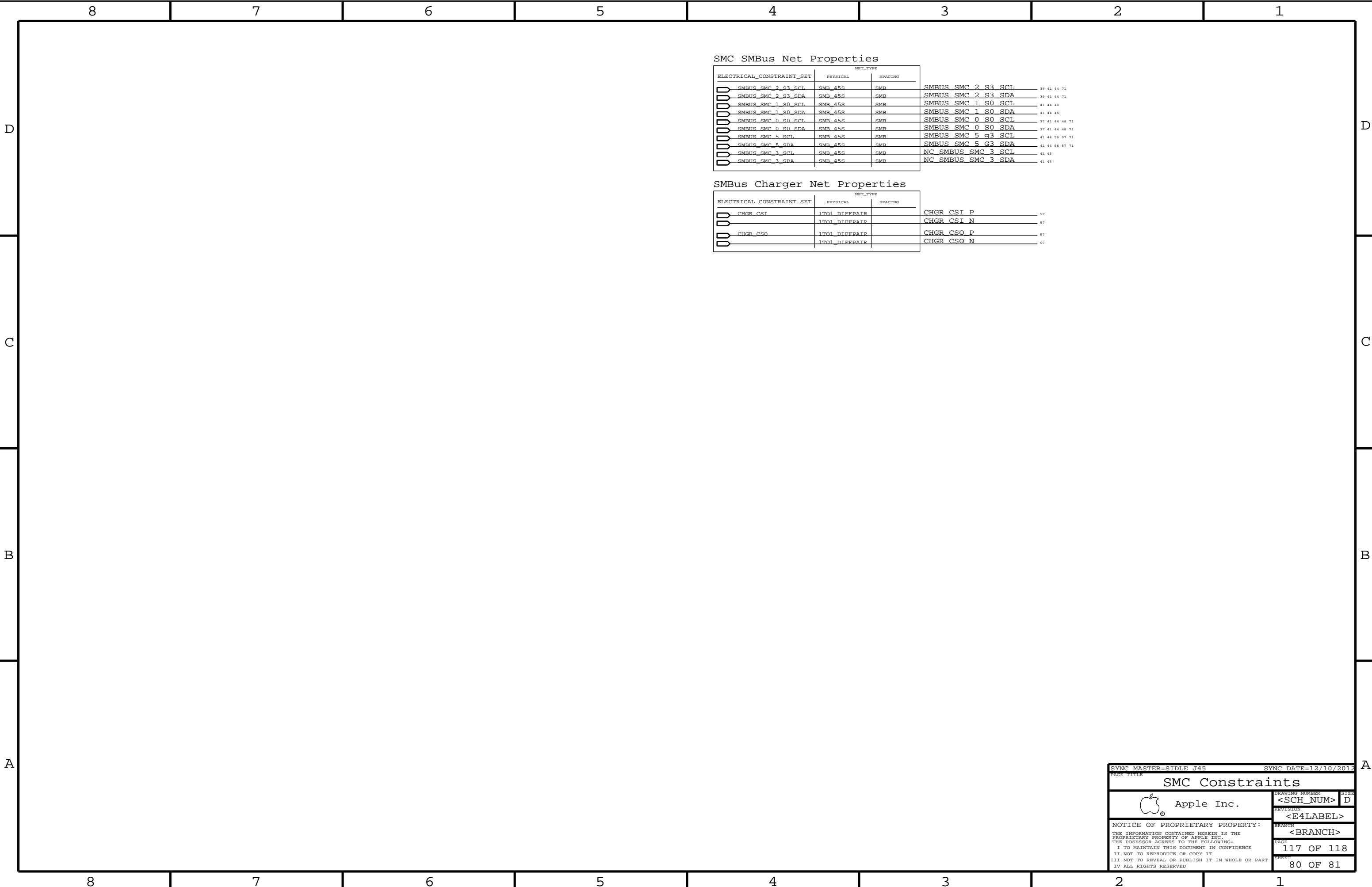
Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND











Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 36 37
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 36 37
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 36 37
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 36 37
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 36 37
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 36 37
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 36 37
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 36 37
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 36 37
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 36 37
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 36 37
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 36 37
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 36 37
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 36 37
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 36 37
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 36 37
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 37 71
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 37 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 36 37
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 36 37
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 37 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 37 71
PPIV35_CAM		S2_MEM_PWR	PPIV35_CAM 36 37
PPOV675_CAM_VREF		S2_MEM_PWR	PPOV675_CAM_VREF 36 37
PPOV675_MEM_CAM_VREFCA		S2_MEM_PWR	PPOV675_MEM_CAM_VREFCA 37
PPOV675_MEM_CAM_VREFDQ		S2_MEM_PWR	PPOV675_MEM_CAM_VREFDQ 37





SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
Camera Constraints			
 Apple Inc.	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
	REVISION		
	<E4LABEL>		
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
BRANCH		<BRANCH>	
PAGE		116 OF 118	
SHEET		79 OF 81	



SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 71
 SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 71
 SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
 SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
 SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
 SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
 SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_S3_SCL	41 44 56 57 71
 SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 71
 SMBUS_SMC_3_SCL	SMB_45S	SMB	NC SMBUS_SMC_3_SCL	41 43
 SMBUS_SMC_3_SDA	SMB_45S	SMB	NC SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 CHGR_CSI	1T01_DIEFPAIR		CHGR_CSI_P	57
 CHGR_CSI	1T01_DIEFPAIR		CHGR_CSI_N	57
 CHGR_CSO	1T01_DIEFPAIR		CHGR_CSO_P	57
 CHGR_CSO	1T01_DIEFPAIR		CHGR_CSO_N	57

SYNC_MASTER=SIDLE_J45

SYNC_DATE=12/10/2012

PAGE_TITLE

SMC Constraints

 Apple Inc.

DRAWING_NUMBER

<SCH_NUM>

SIZE

D

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

REVISION

<E4LABEL>

BRANCH

<BRANCH>

PAGE

117 OF 118

SHEET

80 OF 81

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_50S	*	+1:1_DIFFPAIR	+50_OHM_SR	+50_OHM_SR	+50_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_1T01_50S	*	+1:1_DIFFPAIR	+50_OHM_SR	+50_OHM_SR	+50_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
AUDIODIFF	*	+1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	+1:1_DIFFPAIR	+45_OHM_SR	+45_OHM_SR	+45_OHM_SR	0.2 MM	0.2 MM
THERM_1T01_45S	*	+1:1_DIFFPAIR	+45_OHM_SR	+45_OHM_SR	+45_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
SENSE_1T01_45S	*	+1:1_DIFFPAIR	+45_OHM_SR	+45_OHM_SR	+45_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	+2X_DIELECTRIC	?
THERM	*	+2X_DIELECTRIC	?
AUDIO	*	+2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	+STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P20M	*	0.20 MM	1000
PWR_P20M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P20M
CPU_VCCSENSE	GND	*	GND_P20M

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P20M
GND	PCI_E*	*	GND_P20M
GND	SATA*	*	GND_P20M
USB	GND	*	GND_P20M
CLK_PCIE	SB_POWER	*	PWR_P20M
SB_POWER	SATA*	*	PWR_P20M
USB	SB_POWER	*	PWR_P20M

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_72D	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_37S	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_85D	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
PCIE_85D	*	OVERWRITE	OVERWRITE	0.09 MM	10 MM	OVERWRITE	OVERWRITE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1T01_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPUDDR_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPUDDR_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPU_DDR_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_CPU_DDR_R_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUTHMSNS_D2_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUTHMSNS_D2_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_LCD_PANEL_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_LCD_PANEL_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	DDR3THMSNS_D1_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	DDR3THMSNS_D1_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	FINTHMSNS_D_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	FINTHMSNS_D_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_N
SENSE	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_R_P
SENSE	SENSE_1T01_45S	SENSE	ISNS_1V35_MEM_R_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_N
SENSE	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_R_P
SENSE	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_R_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKLT_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKLT_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER5V_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER5V_N
SENSE	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER3V3_P
SENSE	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER3V3_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_N
SENSE	SENSE_1T01_45S	SENSE	CPUVR_ISNS_P
SENSE	SENSE_1T01_45S	SENSE	CPUVR_ISNS_N
SENSE	THERM_1T01_45S	THERM	PLV05_GPU_PEX_IOVDD_SNS_P
SENSE	THERM_1T01_45S	THERM	PLV05_GPU_PEX_IOVDD_SNS_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUVR_ISUM_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	CPUVR_ISUM_R_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	GFXIMVP_ISNS1_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	GFXIMVP_ISNS1_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	GFXIMVP_ISNS1_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	GFXIMVP_ISNS1_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P
AUDIO	AUDIODIFF	AUDIO	ISNS_TBT_R_N
AUDIO	AUDIODIFF	AUDIO	ISNS_TBT_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_R_P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	ISNS_SSD_R_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05S0_CS_P
SENSE	THERM_1T01_45S	THERM	PLV05S0_CS_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	PLV05S0_SENSE_P
SENSE	THERM_1T01_45S	THERM	PLV05S0_SENSE_N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_THERMD_P
SENSE	THERM_1T01_45S	THERM	TBT_THERMD_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P
AUDIO	AUDIODIFF	AUDIO	CHGR_CSI_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P
AUDIO	AUDIODIFF	AUDIO	CHGR_CSO_R_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_R_P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_S2_R_N

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P
AUDIO	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N
AUDIO	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P
AUDIO	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N
AUDIO	AUDIODIFF	AUDIO	RSUBIN_P
AUDIO	AUDIODIFF	AUDIO	RSUBIN_N
AUDIO	AUDIODIFF	AUDIO	LSUBIN_P
AUDIO	AUDIODIFF	AUDIO	LSUBIN_N
AUDIO	AUDIODIFF	AUDIO	AUD_LO2_R_P
AUDIO	AUDIODIFF	AUDIO	AUD_LO2_R_N
AUDIO	AUDIODIFF	AUDIO	AUD_LO2_L_P
AUDIO	AUDIODIFF	AUDIO	AUD_LO2_L_N
AUDIO	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P
AUDIO	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N
AUDIO	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P
AUDIO	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N
AUDIO	AUDIODIFF	AUDIO	SPKRAMP_RIN_P
AUDIO	AUDIODIFF	AUDIO	SPKRAMP_RIN_N
AUDIO	AUDIODIFF	AUDIO	SPKRAMP_LIN_P
AUDIO	AUDIODIFF	AUDIO	SPKRAMP_LIN_N
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P
AUDIO	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N
AUDIO	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P
AUDIO	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N
AUDIO	DIFFPAIR	AUDIO	CODEC_HS_MIC_P
AUDIO	DIFFPAIR	AUDIO	CODEC_HS_MIC_N
AUDIO	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P
AUDIO	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N
AUDIO	DIFFPAIR	AUDIO	AUD_HS_MIC_P
AUDIO	DIFFPAIR	AUDIO	AUD_HS_MIC_N
AUDIO	DIFFPAIR	AUDIO	HS_MIC_P
AUDIO	DIFFPAIR	AUDIO	HS_MIC_N
AUDIO	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P
AUDIO	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N
AUDIO	AUDIODIFF	AUDIO	AUD_LO3_R_P
AUDIO	AUDIODIFF	AUDIO	AUD_LO3_R_N
AUDIO	AUDIODIFF	AUDIO	AUD_LO3_L_P
AUDIO	AUDIODIFF	AUDIO	AUD_LO3_L_N
SB_POWER			PP3V3_S5
SB_POWER			PP3V3_S0
SB_POWER			PP1V35_S3RS0_CPUDDR
GND			GND

Project Specific Constraints

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SYNC MASTER=SIDLE J45

SYNC DATE=12/10/2012

DRAWING NUMBER
<SCH_NUM>

REVISION
<E4LABEL>

BRANCH
<BRANCH>

PAGE
118 OF 118

SHEET
81 OF 81